# Design and Metrological Validation of a Programmable High-Voltage I–V Measurement System for Dielectric Breakdown Kinetics


## ABSTRACT

Accurate distinction between intrinsic dielectric breakdown and instrument-induced compliance artifacts is a fundamental challenge in semiconductor reliability metrology. Addressing this requirement, this paper presents the design and metrological verification of a programmable high-voltage (HV) I–V measurement system optimized for breakdown kinetics analysis. The architecture integrates a ramp-controlled HV source with a dual-channel, galvanically isolated data acquisition module, achieving an effective post-processed noise floor in the sub-nA range to ensure signal integrity across the full dynamic range. A central contribution is the validation of a compliance-aware detection strategy. By localizing the intrinsic Hard Breakdown (HBD) onset at the global maximum of the differential slope ($|dI/dV|$) and explicitly excluding the subsequent Compliance-Limited Region (CLR), this approach eliminates ambiguity in parameter reporting. Experimental verification on 150-nm $Si/SiO_2$ MOS capacitors demonstrates the system's capability to resolve field-dependent leakage, identifying mixed Fowler–Nordheim and Poole–Frenkel conduction mechanisms with high linearity ($R^2 > 0.97$) within a 2–7 MV/cm diagnostic window. Furthermore, the study reports a mean breakdown field of 6.38 MV/cm with a coefficient of variation of 15.7% ($n = 6$), validating the platform as a transparent and reproducible solution for rigorous dielectric integrity studies and failure analysis.



**Keywords:** *High-voltage instrumentation, dielectric breakdown, compliance-limited breakdown, MOS reliability, metrological verification.*


## 1. INTRODUCTION

The continuous scaling of metal-oxide-semiconductor (MOS) technologies imposes increasingly stringent requirements on the reliability of gate dielectrics. This challenge is not limited to conventional Silicon devices but is even more critical in emerging wide-bandgap power devices like SiC MOSFETs, where gate oxide integrity remains a primary reliability concern [1]. As device dimensions shrink, the electric field across the oxide layer intensifies, making the accurate characterization of dielectric breakdown (BD) mechanisms critical for predicting device lifetime [2]–[6]. Understanding the degradation kinetics—ranging from trap-assisted tunneling in the pre-breakdown regime to the catastrophic hard breakdown (HBD) event—necessitates precise current–voltage (I–V) and time-dependent dielectric breakdown (TDDB) measurements under high-field stress [5], [7]. Conventionally, dielectric characterization is performed using commercial semiconductor parameter analyzers (SPAs), which are optimized for high-precision, general-purpose measurements. However, the centralized architecture of standard ATEs can present challenges when implementing highly specific, dynamic stress protocols tailored to breakdown kinetics, particularly regarding cost-efficiency and real-time feedback flexibility [8]. Consequently, the development of custom programmable instrumentation has emerged as a viable approach to bridge the gap between metrological rigour and the adaptability required for advanced reliability studies.

A critical metrological aspect of high-voltage breakdown testing involves the interaction between the device under test (DUT) and the instrument's compliance setting. As demonstrated in studies regarding breakdown evolution, the external circuit impedance and power dissipation limits directly influence the stability and morphology of the resulting conducting filament [9]–[11]. Consequently, during a hard breakdown (HBD) event, the current rises abruptly until clamped by the compliance limit, yielding a measured transient that convolves the intrinsic breakdown mechanism with a subsequent Compliance-Limited Region (CLR) [12]. Accurately distinguishing these regimes is essential for determining the true energy dissipated during failure. However, because general-purpose instrumentation typically captures the aggregate response, the automated separation of the intrinsic onset from compliance artifacts necessitates dedicated algorithmic post-processing to mitigate potential ambiguity in post-breakdown characterization.

Recent developments in instrumentation have explored custom I–V tracers to address specific characterization needs, ranging from large-scale

cryogenic CMOS analysis [13] to the rigorous evaluation of wide-bandgap power devices [14]. Yet, many existing solutions prioritize cost reduction over metrological rigor, often lacking the dynamic range required to resolve low-level leakage currents—a critical parameter for modeling carrier trapping behavior [14]—while simultaneously handling high-energy breakdown transients common in high-voltage applications [15]. Furthermore, distinguishing valid breakdown events from system background noise often necessitates advanced data filtering and trigger validation algorithms [16]. Consequently, the integration of intelligent detection strategies capable of identifying the precise physical onset of breakdown, independent of hardware latency, remains an area requiring further advancement in measurement science.

This paper reports the design, implementation, and metrological validation of a programmable high-voltage I–V measurement system optimized for dielectric breakdown kinetics. Unlike basic data loggers, the proposed architecture emphasizes measurement integrity through galvanic isolation and a high-dynamic-range sensing topology utilizing precision voltage dividers. A central contribution of this work is the development of a compliance-aware detection strategy that mathematically discriminates between the physical HBD event and the artifactual CLR. This ensures that reported breakdown parameters reflect true material limits rather than instrument constraints.

The validation of the proposed system is performed on 150 nm Si/$SiO_2$ MOS capacitors. The study demonstrates the instrument's capability to: (i) resolve pre-breakdown conduction mechanisms, including Fowler–Nordheim (FN) and Poole–Frenkel (PF) emission; and (ii) accurately extract the breakdown field ($E_{bd}$) and charge-to-breakdown ($Q_{bd}$) by explicitly excluding compliance artifacts. By bridging the gap between flexible hardware design and rigorous metrological analysis, this work provides a transparent and robust platform for advanced dielectric reliability studies.

## 2. MATERIALS AND METHODS

### 2.1. Device under test (DUT) and dielectric physics

The measurement system was validated using planar Si/$SiO_2$ metal–oxide–semiconductor (MOS) capacitor structures featuring a nominal gate-oxide thickness of $t_{ox} = 150$ nm and a lithographically defined effective active area of $A_{eff} = 1.0 \times 10^{-4}$ cm$^2$ (nominally $100 \times 100$ $\mu$m$^2$). In gate-oxide reliability metrology, the oxide electric field $E_{ox}$ serves as the primary stress variable [17], [18]. Within the pre-breakdown regime, where the oxide impedance dominates the external series network ($Z_{ox} \gg R_{lim} + R_{series}$), the field is approximated by:

$$E_{ox}(t) \approx \frac{V_{DUT}(t)}{t_{ox}} \text{ [V/cm]}, \quad (1)$$

and the current density is calculated as:

$$J(t) = \frac{I_{DUT}(t)}{A_{eff}}. \quad (2)$$

These definitions are applied consistently for both conduction-mechanism diagnostics and breakdown reporting. Metrologically, the measured I–V response is interpreted across three regimes: (i) pre-breakdown leakage governed by field-assisted transport; (ii) hard breakdown (HBD) onset associated with an abrupt collapse of dielectric impedance; and (iii) a Compliance-Limited Region (CLR), i.e., a post-breakdown trajectory governed primarily by the external limiting path and source compliance rather than intrinsic oxide physics. Because the CLR is instrument-dependent, explicitly separating the intrinsic HBD onset from this region is essential to ensure reported breakdown parameters remain material-relevant and comparable [19].

### 2.2. Measurement system architecture and data acquisition

The HV I–V tracer comprises a DC high-voltage source (G) with a series current-limiting resistor $R_{lim}$, a contacting fixture housing the DUT (represented by the Si–$SiO_2$ equivalent network), and a galvanically isolated two-channel oscilloscope operated in X–Y acquisition mode (Figure 1). In the experiments, the stress was applied as a quasi-linear monotonic ramp by slowly adjusting the source control knob. Instead of assuming a nominal slew rate from the source setting, the effective ramp rate was quantified directly from the measured $V_{DUT}(t)$ trace in the pre-breakdown region, which also provides an internal consistency check of ramp monotonicity and repeatability.

The instantaneous loop balance can be expressed in lumped form as:

$$V_{source}(t) = V_{DUT}(t) + I(t)R_{lim} + I(t)R_{series}, \quad (3)$$

where $R_{series}$ aggregates the contact, wiring, and fixture resistances within the contacting device (Figure 1). In the pre-breakdown regime, the leakage current is sufficiently low such that $I(t)(R_{lim} + R_{series}) \ll V_{DUT}(t)$, justifying

$V_{DUT} \approx V_{source}$ for field extraction. After breakdown, the DUT impedance collapses and the voltage drop shifts predominantly to the external limiting path, producing the characteristic instrument-governed CLR trajectory.

*Voltage channel (A1):* The DUT voltage is acquired between nodes X4–X5 and scaled by a precision divider $R_{D1}$ (1:10) prior to digitization on Channel A1, yielding:

$$V_{DUT}(t) = k_V\, V_{A1}(t),\ k_V = 10. \qquad (4)$$

*Current channel (A2):* The DUT current is reconstructed from a dedicated current-monitor node (X3 in Fig.~1) routed to Channel A2 through divider $R_{D2}$ (1:100). Rather than relying on a single component-level assumption (e.g., a standalone shunt), the absolute current is obtained using an end-to-end calibrated transfer coefficient that captures the complete measurement chain (monitor node scaling, divider ratio, input loading, and digitizer scaling):

$$I_{DUT}(t) = k_I\, V_{A2}(t). \qquad (5)$$

Both oscilloscope inputs present high impedance loading ($R_{A1} = R_{A2} = 1$ MΩ, Figure 1), minimizing disturbance of the divider networks. The I–V characteristic is formed by pairing synchronous samples $\{V_{DUT}(t), I_{DUT}(t)\}$ recorded during the ramp, with X–Y mode providing a direct visualization of the trajectory while the time-stamped traces are retained for subsequent parameter extraction.

*Effective resolution and analysis decade:* The leakage-analysis and regression reported in this study are confined to the current-density decade $|J| = 10^{-6}$–$10^{-5}$ A/cm$^2$. With $A_{eff} = 10^{-4}$ cm$^2$, this corresponds to $I_{DUT} \approx 0.1$–$1$ nA. The instrument "floor" relevant to fitting is therefore defined as an effective post-processed resolution, obtained after synchronous acquisition and the same time-domain conditioning used in the analysis pipeline (Section 2.3), rather than the instantaneous peak-to-peak noise of raw, unfiltered traces. Under this definition, the effective regression floor was verified to be in the sub-nA range, ensuring that the selected best-decade window remains above the analysis-relevant floor.

### 2.3. Compliance-Aware breakdown detection and parameter extraction

Breakdown parameters are extracted automatically from the acquired time-series data to eliminate subjective manual interpretation and to prevent misidentifying CLR artifacts as intrinsic breakdown events [20]. The detection pipeline first applies a 5-point moving median filter to suppress isolated spikes without distorting the breakdown edge. A valid breakdown event is then identified using a composite criterion: (i) the current must exceed a conservative threshold $I_{th}$ (set above the effective analysis floor), and (ii) within this gated segment, the intrinsic breakdown time $t_{bd}$ is localized at the global maximum of the differential slope:

$$\left.\frac{dI}{dV}\right|_i \approx \frac{I_{i+1} - I_{i-1}}{V_{i+1} - V_{i-1}},\ t_{bd} = \arg\max_i \left|\frac{dI}{dV}\right|_i. \qquad (6)$$

Accordingly, the breakdown voltage and field are reported as:

$$V_{bd} = V_{DUT}(t_{bd}),\ E_{bd} = \frac{V_{bd}}{t_{ox}}. \qquad (7)$$

Importantly, $V_{bd}$ is extracted from the measured $V_{DUT}(t)$ (Channel A1 reconstruction) rather than the source command, avoiding ambiguity once series drops become non-negligible immediately after impedance collapse. Furthermore, the injected charge-to-breakdown is computed by integrating the current only up to the intrinsic failure point:

$$Q_{bd} = \int_0^{t_{bd}} I_{DUT}(t)\, dt,\ Q_{bd,\mathrm{dens}} = \frac{Q_{bd}}{A_{eff}}. \qquad (8)$$

This definition strictly isolates the pre-breakdown stress history from the post-breakdown CLR, which is treated as an extrinsic, instrument-governed response [21].

### 2.4. Conduction mechanism diagnostics

To verify that the tracer resolves physical charge transport rather than digitization artifacts, leakage data are analyzed within a standardized diagnostic window, typically $E_{ox} \in [2,7]$ MV/cm, explicitly excluding CLR samples. The data are transformed into canonical Fowler–Nordheim (FN) coordinates [22]:

$$\ln\left(\frac{J}{E^2}\right) = \ln(A_{FN}) - \frac{B_{FN}}{E}, \qquad (9)$$

where $A_{FN}$ and $B_{FN}$ are physical coefficients related to the effective barrier height and carrier mass (with $E$ expressed in V/cm). In addition, Poole–Frenkel (PF) behavior is examined via the linearity of $\ln(J/E)$ versus $\sqrt{E}$ [23]. For comparability across devices and to avoid both floor-limited samples and near-breakdown fluctuations, regression is restricted to the most linear single-decade subset constrained to $|J| = 10^{-6}$–$10^{-5}$ A/cm$^2$ ("best non-floor decade"). Within this window, $R^2$ values are reported together with extracted slopes as objective metrics

of transport-consistency. These linearizations are used as a metrological consistency check (confirming structured field dependence above the effective analysis floor), rather than as exclusive proof of a single microscopic transport mechanism.

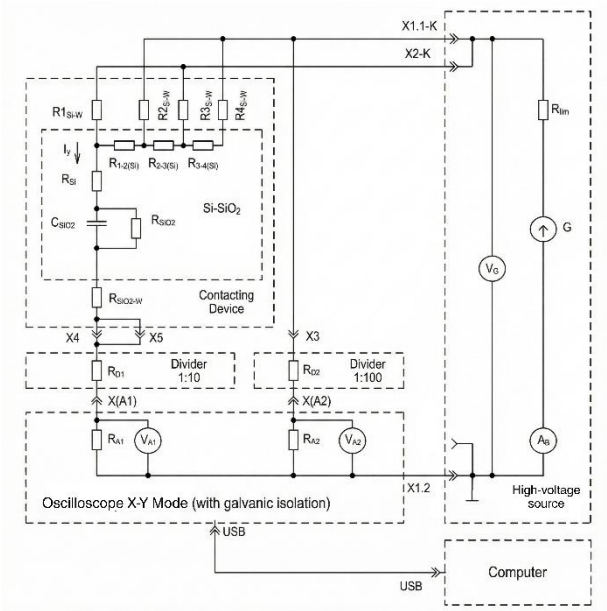


**Figure 1**. Schematic diagram of the programmable high-voltage I–V measurement system. The setup integrates a computer-controlled high-voltage source, a contacting device housing the $Si/SiO_2$ DUT (represented by its electrical equivalent circuit), and a galvanically isolated oscilloscope for data acquisition. Precision resistive dividers ($R_{D1}$ and $R_{D2}$) are utilized to scale the device voltage ($V_{A1}$, 1:10 ratio) and current-sensing signal ($V_{A2}$, 1:100 ratio) to match the digitizer's input range.

## 3. RESULTS AND DISCUSSION

### 3.1. Simulation-Guided verification of the breakdown signature

Prior to experimental characterization, the expected electrical fingerprint of oxide breakdown under a monotonic voltage ramp was verified using a compact SPICE-level representation of the $Si/SiO_2$ MOS structure coupled with the external limiting network [24],[25]. For clarity of signature identification, the pre-breakdown leakage branch in the model was deliberately minimized, ensuring that the transition is dominated by the impedance collapse event rather than by an assumed leakage law.

The simulated I–V response (Figure 2) exhibits two clearly distinguished regimes: an initial high-impedance insulating region, followed by an abrupt hard breakdown (HBD) transition. Crucially, once the DUT collapses into a low-impedance state, the post-event current is no longer governed by intrinsic oxide transport. Instead, the trajectory transitions into a Compliance-Limited Region (CLR), where the measured current is determined primarily by the external protection path (specifically the limiting resistor $R_{lim}$) and the continuing increase of the applied source voltage [26].

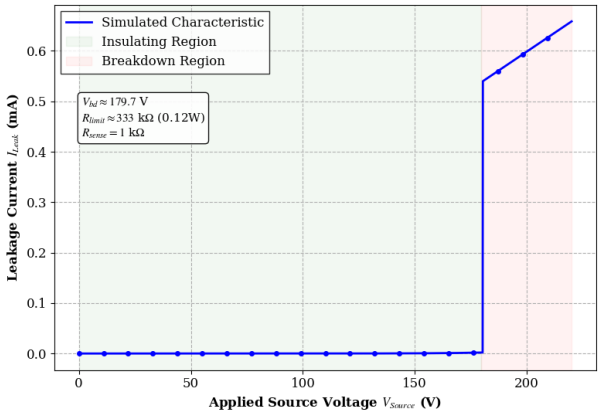


**Figure 2.** SPICE-simulated I–V characteristic illustrating the protection concept. A hard-breakdown transition occurs at an illustrative voltage $V_{bd} \approx 179.7$ V, followed by a linear Compliance-Limited Region (CLR) governed by the external limiter ($R_{lim} \approx 330$ kΩ), distinct from intrinsic oxide physics.

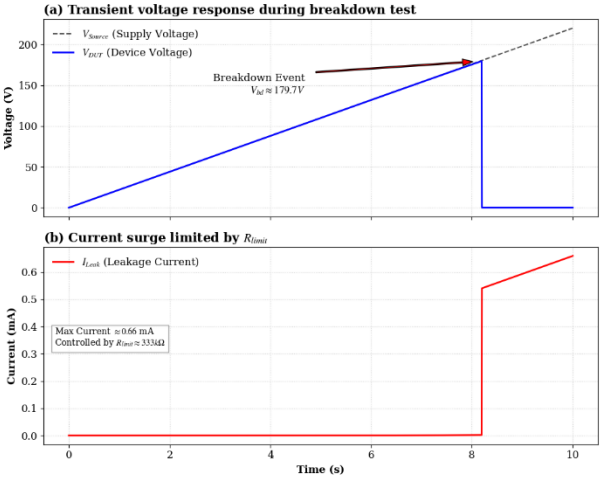


**Figure 3.** Simulated transient breakdown signatures. (a) $V_{DUT}$ follows $V_{source}$ up to breakdown, then collapses rapidly toward zero. (b) The post-event current surge is immediately clamped by $R_{lim}$, validating the limiter-governed CLR fingerprint used to separate intrinsic HBD onset from the instrument/network response.

The transient waveforms presented in Figure 3 further elucidate this mechanism. As shown in Figure 3(a), the device voltage $V_{DUT}$ tracks the source ramp $V_{source}$ up to the breakdown instant —simulated here at an illustrative threshold of $V_{bd} \approx 179.7$ V—before collapsing rapidly toward zero, indicating the loss of dielectric integrity. Concurrently (Figure 3(b)), the resulting current

surge is immediately clamped by the external limiter ($R_{lim} \approx 330$ kΩ), validating the protection concept. This confirms that the post-breakdown segment represents an instrument/network-determined response rather than intrinsic material physics. Consequently, for all subsequent experimental analyses, the breakdown field $E_{bd}$ is extracted at the intrinsic transition point (defined by the global maximum of $|dI/dV|$), while the subsequent CLR is explicitly excluded from transport interpretation. Note that the breakdown threshold in the simulation is strictly illustrative for signature separation and is not tuned to match the specific $E_{bd}$ values of the fabricated samples.

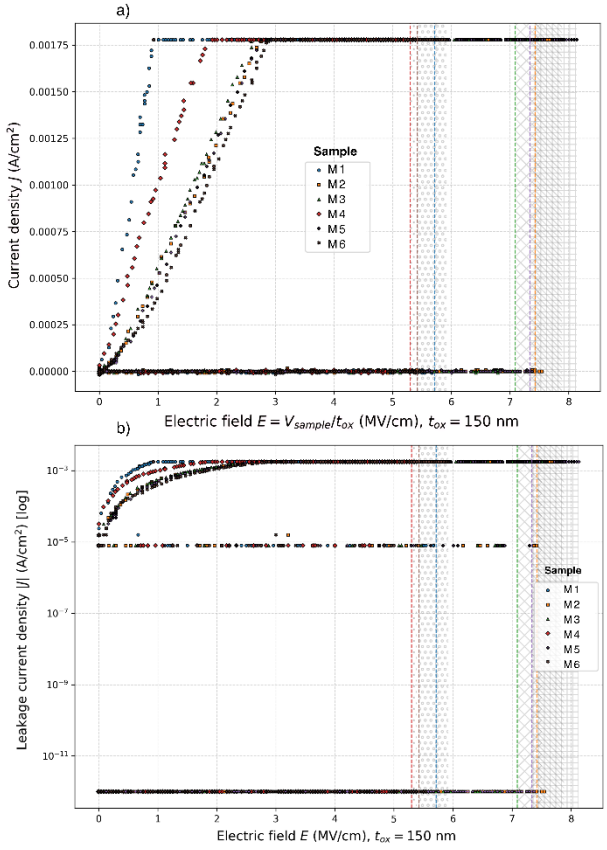


**Figure 4.** Baseline Si/$SiO_2$ breakdown characteristics ($t_{ox} = 150$ nm) for samples M1–M6. (a) Linear $J - E$ overlays; vertical dashed lines mark $E_{bd}$ extracted at the intrinsic transition (global maximum of $|dI/dV|$). The hatched high-field band denotes the Compliance-Limited Region (CLR) governed by the external limiter and thus excluded from physics-based analysis. (b) Semi-log $|J| - E$ overlays highlighting the pre-breakdown leakage branch; resolution-limited floor points are shown for visualization but are excluded from fitting.

### 3.2. Experimental I–V characteristics of baseline Si/$SiO_2$ devices

Figure 4 consolidates the experimental breakdown measurements of the baseline sample set (M1–M6). The characteristics are presented as linear $J - E$ overlays (Figure 4a) and semi-log $|J| - E$ overlays (Figure 4b), with the oxide field computed consistently as $E = V_{DUT}/t_{ox}$ ($t_{ox} = 150$ nm). Across all devices, the traces exhibit the expected three-regime evolution: (i) field-dependent pre-breakdown leakage; (ii) abrupt impedance collapse at the breakdown onset; and (iii) a post-event trajectory corresponding to the limiter-governed CLR (indicated by the hatched region).

In the semi-log representation (Figure 4b), the data reveals a clear separation between quantization-limited noise at very low currents (appearing as a horizontal floor cluster) and the structured, field-dependent leakage branch that rises with increasing field prior to breakdown. To ensure metrological rigor, all conduction diagnostics and mechanism checks in this work are performed exclusively on non-floor samples–defined as data points that exceed the effective post-processed resolution threshold and remain strictly within the pre-breakdown regime.

The breakdown field $E_{bd}$ is operationally assigned to the intrinsic transition point corresponding to the global maximum of $|dI/dV|$. The extracted $E_{bd}$ values are marked by vertical dashed lines in Figure 4. This definition firmly anchors $E_{bd}$ to the onset of the physical impedance collapse, thereby avoiding bias from the subsequent limiter-governed segment which is excluded from material characterization.

### 3.3. Pre-Breakdown conduction diagnostics

To verify that the recorded pre-breakdown leakage exhibits structured field dependence—rather than being dominated by floor artifacts or post-breakdown limiting—conduction diagnostics were performed using Fowler–Nordheim (FN) and Poole–Frenkel (PF) coordinate linearizations (Figure 5). All transformations utilize magnitude quantities ($|J|$, $|E|$) to facilitate polarity-invariant comparison.

FN diagnostics are evaluated by plotting $\ln(J/E^2)$ versus $1/E$, while PF diagnostics are evaluated by plotting $\ln(J/E)$ versus $\sqrt{E}$. Recognizing that both low-field data (floor-limited) and near-breakdown data (incipient instability) can distort regression analysis, a conservative "best non-floor decade" strategy is enforced. Specifically, for each sample, the regression subset is restricted to the most linear single-decade segment constrained to $|J| = 10^{-6}$–$10^{-5}$ A/cm $^2$. Furthermore, the analysis is strictly limited to points that are (i) unequivocally pre-breakdown and (ii) non-floor (excluding quantization-limited zero/near-zero samples). This methodology ensures that the fitted

slopes reflect resolvable leakage transport rather than digitizer limitations or CLR clipping.

As illustrated in Figure 5, the resulting linearities are high, with coefficients of determination $R^2$ ranging from 0.972 to 0.989 for FN and 0.992 to 0.997 for PF fits. It is emphasized that these linearizations serve primarily as metrological diagnostics to confirm signal integrity and consistency, rather than as exclusive proof of a single microscopic transport mechanism, given that multiple conduction models can appear quasi-linear over restricted field windows in thick oxides.

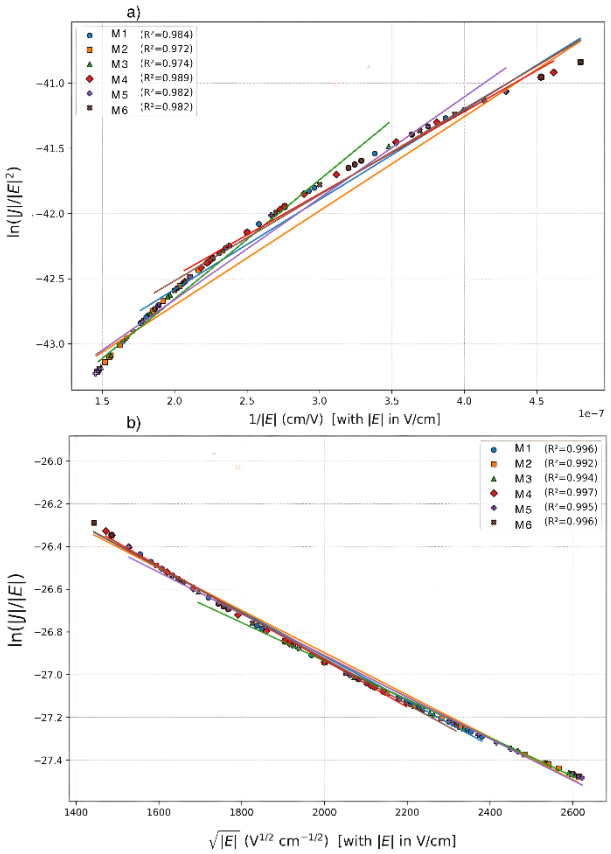


**Figure 5.** Pre-breakdown conduction diagnostics for the baseline set (M1–M6). Linear fits are performed within the pre-breakdown window (2–7 MV/cm) using the "best non-floor decade" $|J| = 10^{-6}$–$10^{-5}$ A/cm $^2$. (a) Fowler–Nordheim coordinates, $\ln(J/E^2)$ versus $1/E$. (b) Poole–Frenkel coordinates, $\ln(J/E)$ versus $\sqrt{E}$. Solid lines represent regressions; $R^2$ values are reported in the legends.

### 3.4. Breakdown statistics and consolidated baseline performance

For the baseline sample set, the extracted breakdown fields span a range of $E_{bd} = 5.30 - 7.42$ MV/cm (Table 1), with a mean of 6.38 MV/cm and a standard deviation of 1.00 MV/cm (Coefficient of Variation $\approx 15.7\%$, $n = 6$). This dispersion is consistent with the stochastic, "weakest-link" nature of dielectric breakdown in thick oxides and does not, by itself, indicate systematic drift within the measurement chain.

Collectively, these baseline results establish a metrologically defensible reference envelope for the proposed system: (i) the intrinsic breakdown onset is cleanly separated from the limiter-governed CLR via the differential slope criterion; (ii) leakage is clearly resolved on a semi-log scale prior to breakdown, with explicit exclusion of floor-limited samples; and (iii) diagnostic fits achieve high linearity when a strict best-decade, non-floor selection strategy is enforced.

**Table 1.** Breakdown field $E_{bd}$ and pre-breakdown diagnostic slope parameters extracted in the 2–7 MV/cm window using non-floor leakage points (best decade $|J| = 10^{-6}$–$10^{-5}$ A/cm $^2$). Note: The PF linearization is used as a consistency/shape descriptor within the selected field window; high $R^2$ is interpreted as repeatable field dependence in resolvable leakage data.

| Sample | $E_{bd}$ (MV/cm) | Best decade $\|J\|$ (A/cm $^2$) | FN slope $B$ ($\times 10^8$ V/m) | PF slope ($\times 10^{-4}$ V $^{-1/2}$ . m $^{1/2}$) |
|---|---|---|---|---|
| M1 | 5.715 | $10^{-6}$ – $10^{-5}$ | 6.873 | -1.043 |
| M2 | 7.423 | $10^{-6}$ – $10^{-5}$ | 7.226 | -0.990 |
| M3 | 7.090 | $10^{-6}$ – $10^{-5}$ | 9.130 | -0.900 |
| M4 | 5.298 | $10^{-6}$ – $10^{-5}$ | 6.304 | -1.100 |
| M5 | 7.340 | $10^{-6}$ – $10^{-5}$ | 7.773 | -0.975 |
| M6 | 5.423 | $10^{-6}$ – $10^{-5}$ | 6.591 | -1.067 |

## 4. CONCLUSION

This paper has reported the design, implementation, and metrological validation of a programmable high-voltage I–V measurement system tailored for dielectric breakdown kinetics. By integrating a ramp-controlled high-voltage source with a galvanically isolated acquisition architecture, the platform achieves an effective post-processed noise floor in the sub-nA range. This sensitivity enables the simultaneous resolution of low-level pre-breakdown leakage currents and catastrophic breakdown transients within a single experimental setup.

A central contribution of this work is the formalization of a compliance-aware detection strategy. By mathematically distinguishing the intrinsic Hard Breakdown (HBD) onset—localized at the global maximum of the differential slope—from the subsequent artifactual Compliance-Limited Region (CLR), the proposed framework eliminates the parameter ambiguity

often associated with general-purpose instrumentation. Experimental verification on 150-nm $Si/SiO_2$ MOS capacitors demonstrated the system's robustness, yielding a mean breakdown field of 6.38 MV/cm with a coefficient of variation of 15.7% ($n = 6$), alongside high-linearity conduction diagnostics ($R^2 > 0.97$) consistent with Fowler–Nordheim and Poole–Frenkel transport models.

Overall, the proposed hardware–software workflow provides a transparent, reproducible, and rigorous alternative to fixed-function commercial testers for reliability-oriented dielectric metrology. Future work will extend this architecture to support Time-Dependent Dielectric Breakdown (TDDB) protocols and to quantify the impact of laser-induced thermal modifications on gate-oxide integrity.

## Conflict of interest

*The author(s) declare no competing interests.*


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# Thiết kế và đánh giá đặc tính đo lường của hệ thống đo I–V cao áp có khả năng lập trình phục vụ nghiên cứu động học đánh thủng điện môi


## TÓM TẮT

Phân biệt chính xác giữa hiện tượng đánh thủng điện môi thực và các tín hiệu giả do cơ chế giới hạn dòng của thiết bị gây ra là một thách thức cơ bản trong đo lường độ tin cậy bán dẫn. Để giải quyết yêu cầu này, bài báo trình bày thiết kế và thẩm định đặc tính đo lường của một hệ thống đo I–V cao áp khả trình, được tối ưu hóa cho phân tích động học đánh thủng. Kiến trúc hệ thống tích hợp nguồn cao áp điều khiển dạng dốc với mô-đun thu thập dữ liệu hai kênh được cách ly về điện, đạt mức nhiễu nền hiệu dụng sau xử lý ở ngưỡng dưới nA (sub-nA), đảm bảo tính toàn vẹn tín hiệu trên toàn bộ dải động. Đóng góp trọng tâm là việc chuẩn hóa chiến lược phát hiện nhận biết giới hạn dòng: định vị điểm khởi phát đánh thủng cứng (HBD) tại cực đại độ dốc vi phân ($|dI/dV|$) và loại trừ vùng giới hạn dòng (CLR) giả tạo. Thực nghiệm trên tụ MOS Si/$SiO_2$ 150 nm xác nhận khả năng phân giải cơ chế dẫn điện Fowler–Nordheim/Poole–Frenkel ($R^2 > 0.97$) và xác định trường đánh thủng trung bình 6.38 MV/cm (biến thiên 15.7%), khẳng định độ tin cậy của hệ thống cho các nghiên cứu độ bền điện môi nghiêm ngặt.



**Từ khóa:** *Thiết bị đo lường cao áp, đánh thủng điện môi, đánh thủng giới hạn dòng, độ tin cậy MOS, kiểm định đo lường.*