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TRƯỜNG ĐẠI HỌC QUY NHƠN

Kỹ thuật ổn định và bù tần số cho thiết kế bộ khuếch đại thuật toán công suất thấp

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TÓM TẮT

Trong bài báo này, chúng tôi trình bày một thiết kế mạch khuếch đại thuật toán (op-amp) công suất thấp sử dụng các kỹ thuật bù Miller thông thường và bù Miller gián tiếp. Đối với op-amp hoạt động ở điện thế thấp, cách tiếp cận g_m/I_D được sử dụng để xác định kích thước bóng bán dẫn trong thiết kế mạch op-amp. Độ lợi, tốc độ tăng thế, biên độ pha, công suất tiêu tán và các thông số khác được xác định trong thiết kế. Để kiểm chứng các tham số của thiết kế, mạch op-amp được mô phỏng trên phần mềm LT-SPICE. Mục đích của nghiên cứu này là so sánh độ lợi và biên độ pha thu được khi sử dụng các kỹ thuật bù tần số khác nhau, từ đó xác định khả năng lựa chọn kỹ thuật bù tần số phù hợp dựa trên một tập hợp các yêu cầu thiết kế cụ thể. Trong nghiên cứu này, chúng tôi cũng sử dụng các ưu điểm khi kết hợp kỹ thuật bù phản hồi gián tiếp với bóng bán dẫn chia độ dài để thiết kế op-amp hiệu suất cao. Tất cả các thiết kế op-amp được thực hiện trên quy trình chế tạo CMOS 180 nanomet.

Từ khóa: *Khuếch đại thuật toán, công suất điện áp thấp, bù gián tiếp, khuếch đại thuật toán CMOS hai tầng.*

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Stability and frequency compensation techniques for low-power operational amplifier design

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ABSTRACT

A low-power operational amplifier (op-amp) circuit with both conventional and indirect Miller compensating techniques is presented in this work. For low-voltage op-amps, the g_m/I_D method is used to calculate transistor size. The gain, slew rate, phase margin, power dissipation, and other parameters of the proposed op-amp were determined. The developed op-amp circuit was simulated in LT-SPICE to check parameter values. The goal of this study was to examine the gain and phase margins obtained using several frequency compensation techniques in order to identify the best one for a given set of design requirements. To create a high performance op-amp, we used split-length transistors combined with indirect feedback compensation. All op-amps were designed in 180 nm CMOS technology.

Keywords: *Op-amp, Low-voltage low-power, Indirect compensation, Two stage CMOS operational amplifier.*

1. INTRODUCTION

The operational amplifier (op-amp) is a very versatile analog circuit that is frequently used in analog and mixed-signal Integrated Circuit (IC) design.[1,2] Op-amps are frequently developed using sub-micron Complementary Metal Oxide Semiconductor (CMOS) technology, for example, nodes 350 nm, 180 nm, and 130 nm. However, there are numerous approaches for designing the op-amp to meet the requirements of various circuits.[3,4] It typically consists of two or more amplification stages that utilize transistors, integrated capacitors, and, in some cases, integrated resistors. All op-amps, however, must have enough open-loop margin of stability in order to be used in a feedback closed-loop design with acceptable frequency response. As a result, the open-loop configuration of an op-amp should have a phase margin (PM) of 45° or greater, which can be accomplished by the use of Miller compensating techniques. To obtain the required stability and frequency responsiveness, many compensating strategies may be used. These compensation strategies may be used singly or in combination.[3]

Frequency compensation is critical for close-loop stability when designing the op-amps that operate the negative feedback connection. Miller compensation is one of the techniques used to enhance the op-amp's stability and frequency response.[5] The Miller effect can be detected in two ways within a MOSFET analog amplifier. To begin, the Miller effect is created by the MOSFET's construction, which has five

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capacitances between its terminals: drain (D), gate (G), source (S), and bulk (B), as illustrated in Figure1. The capacitance difference between the drain and gate terminals (C_{GD}) establishes a feedback connection between the drain and gate terminals. While C_{GD} is often a low capacitance value, it also demonstrates the effect of the amplifier's high-frequency response. Miller capacitance is the name given to the capacitance C_{GD}.[5]

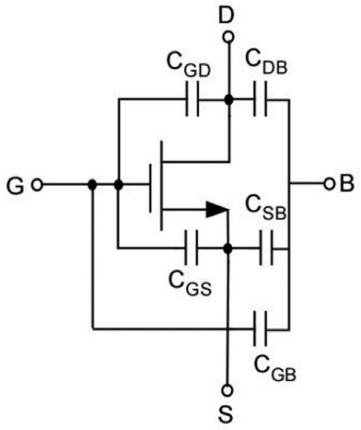

Figure 1. Parasitic capacitances in MOSFET

Second, it can be accomplished by adding an external capacitor (C_c) to the second stage of a standard two-stage CMOS op-amp, as illustrated in Figure 2. A connection between the second stage and the external Miller capacitor (C_c) may be seen in this diagram.

The frequency compensation technique will be demonstrated in this study for the design of operational amplifiers. The direct Miller compensation technique is used in the first design. When comparing the two designs, the indirect Miller compensating technique in conjunction with a split-length transistor is employed in the second design.

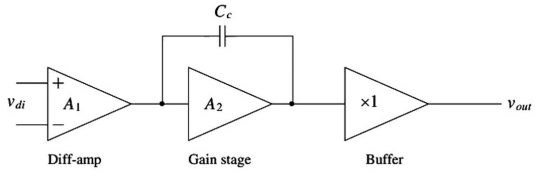

Figure 2. Block diagram of the second voltage amplifier stage with Miller compensation.

Additionally, the Nulling Resistor approach is employed in both designs to boost the efficiency of the operational amplifier. The target amplifier is a two-stage CMOS operational amplifier (op-amp) that operates on a +0.9 V power supply and has high unity gain as well as stability. All simulation investigations were also carried out using the LT-SPICE circuit simulator, which may be found here.

2. DESIGN OF TWO-STAGE OPERATIONAL AMPLIFIER WITH MILLER COMPENSATION

2.1. Design of two stages operational amplifier

Because of its simple structure and robustness, the two-stage CMOS operational amplifier is widely utilized. It also has a high DC gain as well as a wide range of output voltage swings. Transistor M1 and M2 together constitute a differential amplifier, which converts differential voltage to current in the first stage of a two-stage operational amplifier design (Figure 3). This differential current is then sent to the current mirror circuit, which is formed by M3 and M4, which recovers the voltage difference between the two stages. The output of the first stage operational amplifier is essentially identical to the output of the differential voltage amplifier. The M6 is responsible for supplying the differential pair with the bias current I_{B1}. The second stage is comprised of a common source MOSFET amplifier M7, which converts the input voltage of the second stage into current through the use of a MOSFET transistor. The common source transistor is actively loaded with the current sink load M8, which turns the current back into a voltage at the output of the transistor at the same time. Transistor M8 does not provide biasing for transistor M7, and M7 is biased from the gate side of the transistor M8. As a result, the second stage functions similarly to a current sink inverter.

2.2. Miller Compensation

An external Miller capacitor is commonly connected between the output of the second stage and the output of the first stage transistors, as shown in Figure 2.

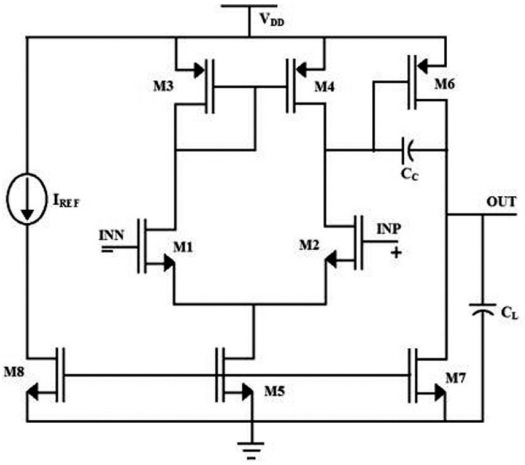

Figure 3. Miller compensated two stage operational amplifier

Figure 4 presents the small-signal model of the two-stage amplifier illustrated in Figure 3, which does not include compensation. When the operational amplifier gain is expressed as a two-pole open-loop transfer function, the result is as follows:[9]

$$\frac{V_{out}}{V_{in}} = A(s) = \frac{A_V}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \quad (1)$$

Where V_{in} represents a small signal differential input voltage. A_V is the op-amp gain and poles p_1 and p_2 are defined by the capacitances linked to the high impedance of the op-amp. In addition, the small-signal equivalent circuit of the two-stage amplifier is shown in Figure 4 when $p_2 >> p_1$, which implies p_1 is the dominant pole. And the small-signal analysis is presented by:

$$A_V = G_{m1}G_{m2}R_1R_2, p_1 = \frac{G_{m1}}{C_1}, p_2 = \frac{G_{m2}}{C_L}$$

A feedback path for an op amp is provided by the

A feedback path for an op-amp is provided by the linked Miller capacitor. The transfer function equation at node V_{in} has an effect on the capacitor C_c, resulting in the following [9]:

$$\frac{V_{out}}{V_{in}} = \frac{R_2R_1G_{m1}G_{m2}\left(1-\frac{sC_c}{G_{m2}}\right)}{\left[\begin{array}{c}1+s\left(C_1R_1+C_2R_2+C_c(R_1+G_{m2}R_1R_2+R_2)\right)\\+s^2R_1R_2(C_cC_2+C_cC_1+C_1C_2)\end{array}\right]} \quad (2)$$

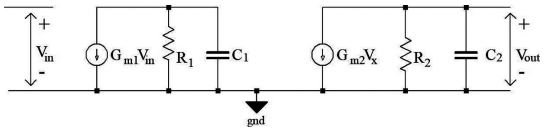

Figure 4. Small-signal model op-amp without compensation

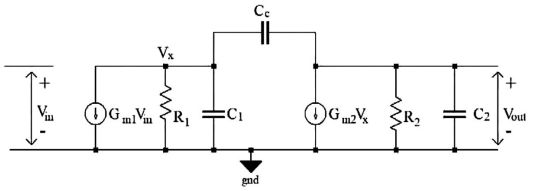

Figure 5. Small-signal model op-amp with compensation

The ratio $V_{out}/V_{in} = G_{m1}R_1G_{m2}R_2$ if s=0. If $s \neq 0$, the Miller effect in the right half plane causes zero transmission in the op-amp:

$$1-\frac{sC_c}{G_{m2}} = 0, p_z = s_z = \frac{G_{m2}}{C_c}$$

The denominator polynomial for an op-amp with two poles is:

$$Y(s) = \left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right) = 1+s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+s^2\left(\frac{1}{p_1p_2}\right) \quad (3)$$

If there is one dominant pole, $p_1 << p_2$ and Y(s) can be:

$$Y(s) = 1+s\left(\frac{1}{p_1}\right)+s^2\left(\frac{1}{p_1p_2}\right) \quad (4)$$

Finding the frequency of the first dominant pole can be done by equating the first and second dominant poles together.

$$p_1 = \frac{1}{R_1C_1+R_2C_2+C_c(G_{m2}R_1R_2+R_1+R_2)} \quad (5)$$

The term $(C_c(G_{m2}\ R_1R_2+R_2+R_1))$ can be realised by connecting it to the first and second stages where C_c is the negative feedback path of the second stage. Moreover, the first term (R_1C_1) is much larger than the second term (R_2C_2) and, usually, C_1 is much smaller than the Miller capacitance. The approximate value of the p_1 is:

$$p_1 = \frac{1}{C_cG_{m2}R_1R_2} \quad (6)$$

The non-dominant pole as the frequency

dominant pole as the frequency of the

of the second pole can be found by equating:

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second pole can be found by equating:

$$p_2 = \frac{C_c G_{m2} R_1 R_2}{R_1 R_2 (C_1 C_2 + C_1 C_c + C_2 C_c)} \quad (7)$$

Meanwhile, $C_1 << C_2$ and $C_1 << C_c$, the approximation of the p_2 can be shown as:

$$p_2 = \frac{G_{m2}}{C_2} \quad (8)$$

The unity gain frequency (UGF) of the two

The unity gain frequency (UGF) of the two-stage amplifier is given by:

$$UGF = \frac{G_{m1}}{C_c} \quad (9)$$

The location of the zero set in the right half-plane in the transfer function and the location of pole-zero is described in Figure 6, (where jw is the imaginary axis and σ is the real axis), it creates a negative phase shift of the amplifier.[5] To achieve the closed-loop gain stability, the location of p_2 and p_z must be at higher frequencies than UGF. If C_c is increased the UGF reduces to approach the stability condition, PM >> 60° and p_2 is located at half of UGF.[3] Moreover, as C_c is increased, p_1 is decreased, and it permits to move p_z further to the right half-plane and p_2 to higher frequencies.

It is shown in Figure 6 that by placing the zero set in the right half-plane of the transfer function and the placement of pole-zero (where jω is the imaginary axis and is the real axis), a negative phase shift is created in amplifier.[5] In order to achieve closed-loop gain stability, the locations of p_2 and p_z must be at frequencies higher than those of the UGF. The UGF decreases until it approaches the stability condition, PM > 60°, and p_2 is positioned at half of the UGF when C_c is increased. Furthermore, as C_c is increased, p_1 decreases, allowing for the displacement of p_z farther to the right half-plane and the expansion of p_2 to higher frequencies.

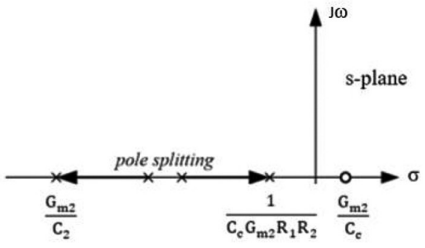

Figure 6. Pole/zero locations

2.3. Procedure of a conventional op-amp design

The conventional design for an operational transconductance amplifier (shown in Figure 3) is based on the large-signal and small-signal device modeling equations when the transistors are operated within the saturation region for power supply of ±0.9 V. The transistor takes after certain conditions, which are called the DC balance conditions as follows:

1. For PM greater than 60°, the second pole (p_2) (or output pole) is considered more significant than 2.2 UGF.

2. First zero is much higher than the second pole, therefore, $p_2 \geq 2.2$ UGF and $z \geq 10$UGF.

3. Assume that $V_{SG4} = V_{SG6}$, this causes "proper mirroring" in the M3-M4 mirror. Furthermore, the gate and drain terminals of the transistor M3 are at the same potential so that transistor M4 is in saturation.

4. Calculate the current for each transistor I_4,I_5,I_6,I_7 according to the square root of drain current (saturation region)[9]

$$\text{If } V_{SG4} = V_{SG6} \qquad I_6 = \frac{W_6}{W_4} I_4 \quad (10)$$

5. When V_{SG5}=V_{SG7}

$$I_7 = \frac{W_7}{W_5} I_5 = \frac{W_7}{W_5} 2I_4 \quad (11)$$

6. For balance, I_6 must equal I_7. This condition is called the "balance conditions".

$$\frac{W_6}{W_4} = \frac{2W_7}{W_5} \quad (12)$$

The op-amp has been designed to operate with a 0.9 V supply. The operational amplifier is designed using the strong inversion region. The transistor dimensions are calculated using the saturation region equation and represent the width and length of each transistor.

3. CALCULATION AND SIMULATION RESULTS

The design parameters of an op-amp with its specifications are given in table 1:

Table 1. The design goal of the operational amplifier

Parameters	Specification
Gain	60dB
Power supply V_{DD}	0.9 V
Gain Bandwidth (GB)	5MHz
Load capacitance C_L	10pF
Slew rate (SR)	10V/μs
Phase margin (PM)	>55°
Input Common Mode Range (ICMR)	0.4V to 0.9V
Power Dissipation	≤ 1mW

We may utilize MOSFETs as small as 180 nm in length (L) and 400 nm in width (W) with the 180 nm technology, but due to the rise in the channel length modulation (λ), we normally do not employ the minimal channel length. It is recommended to utilize $L > 2L_{min}$. Nonetheless, the device length (L) is set to 1 μm in this design and is used throughout the circuit. This value is used to calculate the channel length modulation parameter, which is necessary to calculate the amplifier gain. Following that, to optimize the op-amp's performance, we'll adjust the length of selected MOSFETs while maintaining a constant (W/L). For the calculations, we will use the MOSFET transconductance parameters k_n = 170 $\mu A/V^2$ (for nMOS) and k_p = 36 $\mu A/V^2$ (for pMOS) as input parameters. The saturated drain current i_D in MOSFET is given by:

For nMOS

For nMOS

$$i_D = \frac{1}{2} k_n \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda) \quad (13)$$

For pMOS

For pMOS

$$i_D = \frac{1}{2} k_p \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda) \quad (14)$$

Where channel length modulation is $\lambda = \frac{0.5}{L}$. We use $\lambda = 0.05$ V^{-1} for pMOS and for $\lambda = 0.04$ V^{-1} nMOS in the calculation.

Calculate the value of the compensation capacitor C_c after determining the device length.

$$C_c > \frac{2.2}{10} C_L = 2.2pF$$

C_c were selected as 3pF.

Next, based on the slew rate requirements, determine the minimum value of tail current I_5. The formula used to compute the value of I_5 is.

$$I_5 = \text{SR}.C_c = (3.10^{-12})(10.10^6) = 30\ \mu A$$

Determine the aspect ratio of M3 by following relation, where the threshold voltage is denoted by V_T. Calculate sensitivity S_3 using the equation:

$$S_3 = (W/L)_3$$

$$= \frac{I_5}{k_p[V_{DD} - V_{in}(max) - |V_{T0}|_{(max)} + V_{T1(min)}]^2} \geq 1$$

$$= \frac{30.10^{-6}}{(36.10^{-6})[0.9 - 0.5 - 0.85 + 0.55]^2} = 83$$

Since, M3 and M4 are identical S_3 will be equal to S_4.

$$(W/L)_3 = (W/L)_4 = 83$$

The equation that follows determines the input transistor's transconductance:

$$g_{m1} = GB.C_c.2\pi = (5.10^6)(2\pi)(3.10^{-12}) = 94.25\ \mu s$$

From the above equation, the aspect ratio and M1 and M2 can be directly obtained.

From the above equation, the aspect ratio of M1 and M2 can be obtained as:

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{k_n l_5} = \frac{(94.25\mu)^2}{(170.10^{-6})(30.10^{-6})}$$

$$= 1.74 \sim 2$$

The aspect ratio S_5 and S_6 is determined as:

$$S_5 = (W/L)_5 = \frac{2l_5}{k_n[V_{DS5(sat)}]^2}$$

$$V_{DS5(\text{sat})} = V_{\text{in}\,(min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1(max)} \geq 100\text{mV}$$

$$V_{DS5(sat)} = -0.1 + 0.9 - \sqrt{\frac{30.10^{-6}}{170.10^{-6}.3}} - 0.3 = 0.26\ \text{V}$$

$$S_5 = (W/L)_5 = \frac{2I_5}{k_n[V_{DS5(sat)}]^2} = \frac{2\,(30.10^{-6})}{170.10^{-6}[0.26]^2} = 5.2$$

$S_6 = S_4 \frac{g_{m6}}{g_{m4}}$ with condition $g_{m6} \geq 10 g_{m1} \geq 942.5\mu s$

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} = 60 \frac{942.5\mu}{300\mu} = 188.5$$

The following equation can be used to calculate the

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The following equation can be used to calculate the current via M6.

$$I_6 = \frac{g_{m6}^2}{2k_p S_6} = \frac{(942.5\mu)^2}{2(30.10^{-6})(188.5)} = 78.54\mu\text{A}$$

S_7 should be designed in such a way that the desired current ratios between I_5 and I_6 are achieved:

$$(W/L)_7 = \frac{I_6}{I_5} S_5 = 2.2\frac{78.54\mu}{30\mu} = 5.76$$

Finally determine the value of gain and power dissipation and check its specification.

$$\begin{aligned} P_{\text{diss}} &= (I_5 + I_6)(V_{DD} + |V_{SS}|) \\ &= (30\mu + 78.54\mu)(0.9 + 0.9) \\ &= 0.000195 = 195\ \mu W \end{aligned}$$

To determine A_V

$$\begin{aligned} A_V &= 2\frac{g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)} \\ &= 2\frac{(94.25\mu)(942.5\mu)}{30.1^{-6}(0.04 + 0.05)78.54.10^{-6}(0.04 + 0.05)} \\ &= \frac{9308.83\text{V}}{\text{V}} = 79.8\ dB \end{aligned}$$

All simulations were conducted using typical model process transistor models and the LT-Spice circuit simulator to verify that all design parameters were met, including unity gain frequency (UGF), phase margin (PM), and DC gain.

The results of aspect ratio of each transistor are summarized in Table 2.

Figure 7 illustrates the results of the first op-amp design when various Miller capacitor values are used. As a result of increasing the Miller compensation (increasing the value of C_c), the phase margin has increased, while the unity gain frequency has reduced. In transfer function, the compensation capacitor yields a right-half plane zero.[8] It results in a phase shift toward the negative. The zero-nulling resistor has been used to eliminate this effect (Figure 8).

Table 2. Aspect ratio of each transistor

Transistor	W(μm)	L(μm)	W/L
M_1, M_2	2	1	2
M_3, M_4	83	1	
M_5	5.2	1	5.2
M_6	188.5	1	188.
M_7	5.76	1	5.76

The outcome demonstrates a well-behaved step reaction. When the zero is shifted to the left-half plane (LHP), the zero's phase response is added to the total phase response, thereby increasing the phase margin.

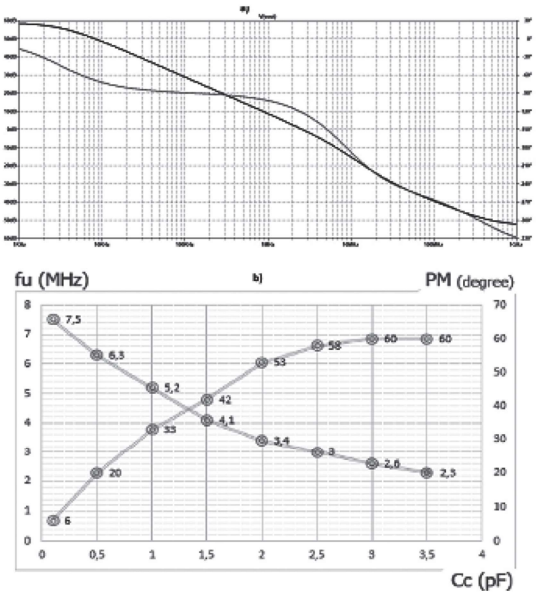

Figure 7. Results for the first op-amp design. a) frequency response of the first op-amp. b) Unity gain frequency and phase margin with different miller capacitor values.

Indirect Miller compensating techniques are used in the second op-amp design. Indirect compensation of the op-amp can be accomplished by cascading the internal low impedance nodes. This node can be built by utilizing the proposed split-length transistor in work.[6]

Figure 9 illustrates the recommended architecture in this article. To prevent the RHP zero, the addition of MOSFETs results in the formation of a common-gate amplifier. The

current I_{Cc} is sent back to the differential op-amp's output via the common-gate MOSFET. Figure 10 illustrates the result of the opamp simulation utilizing the indirect compensation strategy demonstrated in Figure 9.

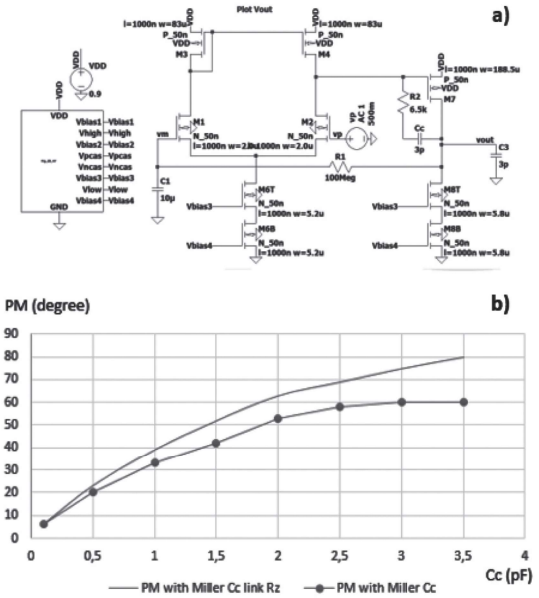

Figure 8. Two-stage op-amp employing miller capacitor and nulling resistor (a) and phase margin with different miller capacitor values (b).

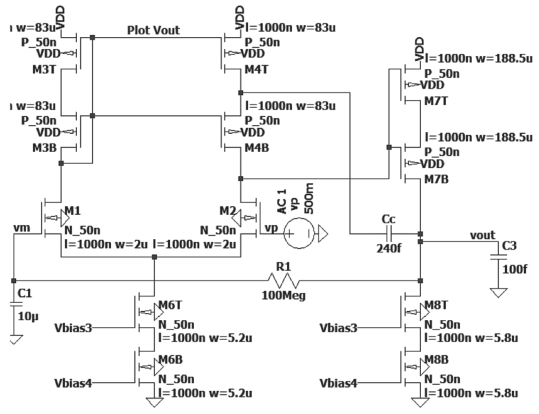

Figure 9. Two-stages op-amp design using Indirect Compensation technique and the split-length transistor.

Because indirect Miller eliminates the initial zero in addition to separating the poles, it speeds up op-amp circuits, adjusts phase margin, and improves UGF.

A comparison of the two operational amplifier designs is shown in Table 3. The DC gain, common mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) have remained constant due to the fact that the input differential pair or current summing branches do not contribute to the PSRR. The UGF is related to power dissipation. The UGF increases with increasing power dissipation. When compared to the previously published work,[7] the power dissipation of the developed operational amplifiers is reduced (Table 3).

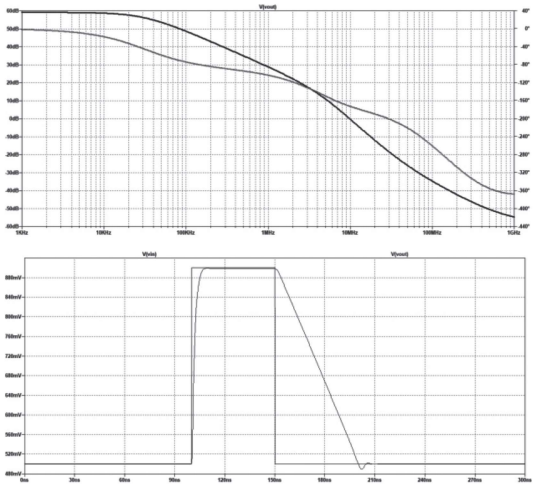

Figure 10. Frequency response and slew rate of op-amp using the indirect compensation with a compensation capacitor of 240 fF.

Table 3. Summary of op-amp simulations

Performance	Reported work [7]	First op-amp	Second op-amp
Power supply (V)	5.0	+0.9	+0.9
Process (µm)	0.35	0.18	0.18
DC gain (dB)	77.25	59	60.2
UGF (MHz)	8.6	2.6	5.7
PM (degree)	53.46	60	57.3
SR (V/µs)	10.4	4.8	7.5
Settling time (ns)	400	234	186
CL (pF)	10	3	3
VOH (V)	3.28	1.2	1.2
VOL (mV)	0	0.2	0.2
ICMR	0.9-3.27	0-1.2	0-1.2
Power dissipation (µW)	480	195	152

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4. CONCLUSION

The paper discusses two op-amp designs with varied gain frequencies and phase margins. Miller (direct) compensation was used to improve the PM; however, the poles were split and a RHP zero was included, resulting in a decrease in the UGF. Additionally, by utilizing split-length transistors for indirect compensation, the PM was corrected and the UGF was enhanced. This design results in a significant increase in the unity gain frequency while keeping an acceptable phase margin, increasing the op-amp's speed and stability.

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