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Các bóng bán dẫn GAAFET và vật liệu 2D cho công nghệ dưới 3 nm: hiệu năng, thách thức chế tạo và chiến lược tích hợp

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TÓM TẮT

Bài báo này nghiên cứu quá trình chuyển đổi từ FinFETs sang Transistor Bao Quanh Cổng (Gate-All-Around Field-Effect Transistors - GAAFETs) như một bước tiến chiến lược cho các nút công nghệ CMOS vượt ngưỡng 3 nm, với trọng tâm là các cải tiến hiệu suất, thách thức chế tạo và chiến lược tích hợp. Chúng tôi thực hiện phân tích so sánh các kiến trúc transistor tiên tiến – bao gồm FinFET 3 nm của TSMC, GAAFET dạng tấm nano 3 nm của Samsung (MBCFET™), và RibbonFET 20A sắp ra mắt của Intel – nhằm làm nổi bật khả năng điều khiển điện trường và dòng dẫn vượt trội của GAAFETs. Vai trò của các vật liệu tiên tiến như SiGe, các hợp chất III–V, và chất bán dẫn hai chiều (ví dụ: MoS- đơn lớp và WSe-) được phân tích trong bối cảnh mở rộng khả năng thu nhỏ xuống dưới 1 nm, đặc biệt là với khả năng giảm thiểu hiệu ứng kênh ngắn. Chúng tôi cũng xem xét các thách thức chế tạo chính liên quan đến công nghệ dưới 3 nm, bao gồm giới hạn của quang khắc EUV, nhu cầu kiểm soát quy trình ở cấp nguyên tử và chi phí sản xuất leo thang. Bên cạnh đó, các kỹ thuật tích hợp dị thể như thiết kế chiplet và xếp chồng 3D được đề xuất như những cách tiếp cận bổ sung để duy trì xu hướng cải thiện hiệu suất. Cuối cùng, chúng tôi thảo luận về các kiến trúc thiết bị sau GAAFET đầy triển vọng – bao gồm CFETs (Transistor bổ sung) và VTFETs (Transistor truyền dọc) – nhấn mạnh nhu cầu đổi mới liên ngành để duy trì quỹ đạo của định luật Moore. Những kết quả thu được cung cấp một góc nhìn toàn diện về việc thu nhỏ thiết bị bán dẫn trong thời đại "<3 nm", với sự cân bằng giữa hiệu suất, hiệu quả năng lượng và khả năng sản xuất.

Từ khóa: *GAAFET, FinFET, vật liệu hai chiều, quang khắc EUV, định luật Moore.*

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GAAFETs and 2D materials for sub-3 nm nodes: performance, fabrication challenges, and integration strategies

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ABSTRACT

This paper investigates the transition from FinFETs to Gate-All-Around Field-Effect Transistors (GAAFETs) as a strategic advancement for CMOS technology nodes beyond 3 nm, with a focus on performance enhancements, fabrication challenges, and integration strategies. We conduct a comparative analysis of state-of-the-art transistor architectures—namely TSMC's 3 nm FinFET, Samsung's 3 nm nanosheet GAAFET (MBCFET™), and Intel's upcoming 20A RibbonFET—to highlight the superior electrostatic control and drive current offered by GAAFETs. The role of emerging materials such as SiGe, III–V compounds, and two-dimensional (2D) semiconductors (e.g., monolayer MoS_2 and WSe_2) is examined in the context of extending transistor scaling into the sub-1 nm regime, particularly with respect to their potential to mitigate short-channel effects. We further address key fabrication challenges associated with sub-3 nm technologies, including the limitations of extreme ultraviolet (EUV) lithography, the need for atomic-scale process control, and escalating production costs. In addition, we explore heterogeneous integration techniques, such as chiplet-based design and 3D stacking, as complementary approaches to sustain performance scaling. Finally, we discuss prospective post-GAAFET device architectures—including Complementary FETs (CFETs) and Vertical Transport FETs (VTFETs)—emphasizing the necessity of cross-disciplinary innovation to uphold the trajectory of Moore's Law. The findings present a comprehensive perspective on semiconductor scaling in the "<3 nm" era, balancing trade-offs between performance, energy efficiency, and manufacturability.

Keywords: *GAAFET, FinFET, 2D materials, EUV lithography, Moore's law.*

1. INTRODUCTION

For several decades, CMOS technology scaling followed a consistent trajectory of planar transistor miniaturization. However, by the 22–20 nm technology node around 2011, planar MOSFETs began to encounter severe short-channel effects and increasing leakage currents, which ultimately limited further downscaling.[1,2] The introduction of the tri-dimensional Fin Field-Effect Transistor (FinFET) marked a pivotal transformation in transistor architecture, restoring electrostatic control and enabling continued scaling. Intel commercialized the first FinFET at the 22 nm node in 2012, followed by major foundries such as TSMC and Samsung at the 16/14 nm nodes.[3,4] In a FinFET, the channel adopts a vertical fin structure, and the gate wraps around three sides of the fin, unlike planar FETs

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where the gate contacts only one side. This geometry significantly enhances gate control over the channel, reducing off-state leakage and facilitating transistor scaling down to the 10 nm, 7 nm, and 5 nm nodes while maintaining sufficient drive current and energy efficiency.[5]

As FinFETs approach gate lengths of approximately 5 nm, their inherent physical limitations have become more pronounced. The requirement for a minimum fin width and spacing imposes a quantized and non-continuous channel width, thereby restricting fine-grained width control and drive-current tuning at ultra-scaled dimensions. Moreover, ultra-narrow fins are more susceptible to performance degradation due to increased series resistance and process variability. While multiple fins can be used in parallel to boost drive current, practical constraints on fin count and layout density limit the extent to which this can be scaled. These factors collectively lead to diminishing returns in performance and rising leakage as FinFETs are extended beyond the ~5 nm threshold.[5,6] Consequently, the FinFET architecture is approaching a fundamental scaling barrier, prompting the development of new transistor structures capable of sustaining Moore's Law into the sub-3 nm regime.[7,8]

Gate-All-Around Field-Effect Transistors (GAAFETs) – realized in practice through nanosheet or nanowire architectures – have emerged as the leading candidates for next-generation nodes at 3 nm, 2 nm, and beyond.[6,9] In a GAAFET, the gate completely surrounds the semiconductor channel on all four sides, offering superior electrostatic control compared to FinFETs, which only provide tri-gate coverage. This fully-surrounding gate configuration eliminates exposed channel regions that contribute to leakage in FinFETs. Figure 1 illustrates this structural progression: from planar FETs (gate on one side), to FinFETs (three-sided gate), to GAAFETs (fully wrapped gate). By eliminating the open top of the channel found in FinFETs, GAAFETs more effectively suppress short-channel effects, resulting in sharper transistor switching and significantly reduced off-state leakage.

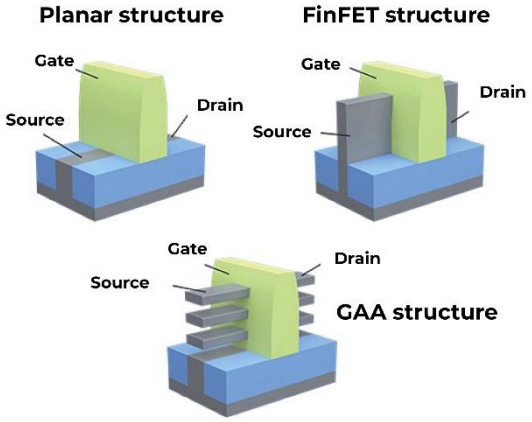

Figure 1. Schematic comparison of transistor architectures: (top-left) planar MOSFET with single-side gate control; (top-right) FinFET with tri-gate coverage; (bottom) gate-all-around (GAA) nanosheet FET in which the metal gate fully surrounds stacked Si/SiGe channels, enabling superior electrostatic control at sub-3 nm nodes. All renderings are to scale for a 16 nm gate length and ~45 nm fin/nanosheet height.

Another key advantage of nanosheet-based GAAFETs is their ability to continuously and independently adjust channel width. In FinFETs, the effective channel width is quantized, as it can only be increased in discrete steps by adding additional fins. In contrast, GAAFETs allow for the stacking of multiple horizontal nanosheet channels, each with customizable width. This architecture enables circuit designers to finely tune drive strength by selecting the number and dimensions of nanosheets.[10,11] Such flexibility allows for optimal balancing of performance and power consumption at the individual device level. Unlike FinFETs—where an intermediate configuration (e.g., 2.5 fins) is physically unattainable – GAAFETs eliminate this granularity constraint, simplifying standard cell library design and potentially improving circuit density and operating speed.

Initial findings from both academia and industry indicate that GAAFETs outperform FinFETs in advanced technology nodes. For

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example, CEA-Leti demonstrated a seven-layer stacked nanosheet GAAFET with nearly 3× higher drive current compared to a conventional two-layer counterpart, emphasizing the benefits of wider effective channel widths through vertical stacking.[12] Likewise, Samsung Electronics reported that its first-generation 3 nm GAA process (MBCFET™) achieved up to 45% reduction in power consumption and a 23% increase in performance compared to its 5 nm FinFET process.[13] These substantial improvements, however, come at the cost of increased fabrication complexity. Stacking nanosheets requires extremely precise atomic-level process control, advanced etching techniques, and in some cases the integration of alternative channel materials such as SiGe to apply strain or engineer specific shapes. As a result, while GAAFETs offer clear scaling advantages, they also present initial challenges in terms of cost and manufacturability. Nevertheless, the transition to GAAFETs is widely regarded as essential for maintaining scaling momentum.

In parallel with structural innovations, researchers are exploring new channel materials to further extend transistor scaling. Silicon, long the cornerstone of the semiconductor industry, faces intrinsic physical limitations at atomic scales, including mobility degradation and quantum confinement effects. Two-dimensional (2D) semiconductors – such as monolayer transition metal dichalcogenides (TMDs) like MoS_2 and WSe_2 - have emerged as promising alternatives due to their atomically thin nature, excellent electrostatics, and favorable carrier mobilities. These materials lack dangling bonds on their surfaces, enabling near-ideal interfaces with gate dielectrics even at sub-nanometer thicknesses.[14] As a result, they offer a viable pathway for scaling gate lengths below 5 nm without incurring severe short-channel effects as observed in silicon-based transistors. Experimental 2D-FETs have demonstrated high on/off ratios and low leakage currents at channel lengths as short as ~1 nm, indicating their potential to extend Moore's Law beyond the material limitations of silicon.[14] However, achieving large-scale, reliable integration of 2D materials into mainstream fabrication processes remains a significant challenge, as further discussed in Section 4.

In addition to device-level advancements, system-level innovations are being pursued to complement and extend the benefits of transistor scaling. As conventional scaling becomes increasingly difficult and cost-prohibitive, heterogeneous integration techniques – such as chiplet-based architectures and 3D stacking – are gaining traction.[15] These strategies aim to improve overall system performance through advanced packaging, for example by dividing a system-on-chip into multiple function-specific chiplets that can be fabricated at optimal nodes and then interconnected, or by vertically integrating logic and memory dies to minimize interconnect delay and energy loss. Even as transistor scaling slows, such integration techniques offer a viable path toward continued performance and efficiency gains.

This paper provides a comprehensive analysis of GAAFET technology and its role in sub-3 nm semiconductor scaling. The key contributions of this work include:

- Comparative evaluation of FinFETs and GAAFETs: We assess performance parameters (e.g., drive current, transconductance), leakage control (e.g., subthreshold swing, DIBL), and design flexibility to highlight the advantages of GAAFETs at advanced nodes.

- Industry case studies: We examine leading-edge 3 nm processes from TSMC (FinFET) and Samsung (GAAFET), and evaluate Intel's roadmap to 2 nm with RibbonFET, focusing on reported gains in power and performance.

- Exploration of 2D materials: We investigate the potential of 2D semiconductors to support scaling into the sub-1 nm regime,

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discussing their benefits and the technical barriers to mass production.

• Fabrication and integration challenges: We analyze key manufacturing constraints at advanced nodes, including EUV lithography limitations, atomic-level variability, and rising wafer costs, and explore heterogeneous integration as a complementary strategy.

• Prospects for future architectures: We consider emerging options beyond GAAFETs—such as Complementary FETs (CFETs) and Vertical Transport FETs (VTFETs)—and emphasize the need for cross-disciplinary research spanning materials, processing, and circuit design to realize next-generation devices.

By addressing these dimensions, this study outlines a strategic roadmap for innovation in semiconductor technologies beyond the 3 nm node, emphasizing how performance, energy efficiency, and manufacturability trade-offs can be effectively navigated over the coming decade.

2. COMPARATIVE ANALYSIS OF FINFETS AND GAAFETS

The transition from FinFETs to GAAFETs is fundamentally motivated by the latter's superior electrostatic control and enhanced design flexibility. This section presents a detailed comparison between FinFET and GAAFET devices across key performance metrics to quantitatively assess these advancements.

2.1. Performance enhancements and electrostatic control

Drive current (ion) and width scaling:

FinFETs facilitated sub-10 nm technology scaling primarily due to their improved gate control compared to planar FETs. However, their drive current capability becomes limited near the 5 nm node due to the quantized nature of channel width imposed by fin geometry.[5,6] A FinFET's effective width is approximated as twice the fin height plus the top width, multiplied by the number of fins. This discrete quantization restricts designers to increase drive current only in fixed increments by adding fins. Figure 2 provides a 3D depiction and cross-sectional comparison of the GAAFET structure.

In contrast, GAAFETs enable continuous width scaling. Through the stacking of multiple nanosheets, the effective channel width – and consequently Ion – can be finely tuned to meet performance demands.[11] Empirical studies have demonstrated that multi-stack GAAFETs can deliver up to a 3× increase in drive current compared to equivalent single- or dual-fin FinFETs, owing to their broader effective channels.[12] This directly translates to enhanced switching speeds and greater current-driving capability in logic cells.

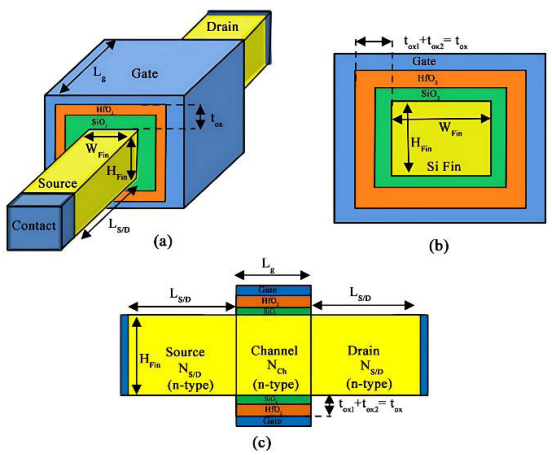

Figure 2. GAAFET nanosheet FET schematics: (a) 3D perspective showing n-type source/channel/drain regions, Si_fin width W_n and height H_n, HfO_2 gate-oxide of thickness t_{ox} surrounding the Si_{fin}, metal gate, and source/drain extensions $L_S/_D$. (b) Top-view cross-section illustrating concentric layers – Si_{fin} (yellow), SiO_2 liner (green), HfO_2 gate-oxide (orange, $t_{ox1} + t_{ox2} = t_{ox}$), and metal gate (blue). (c) Side cross-section perpendicular to the fin, showing channel region (L_g), source/drain doping ($N_S/_D$), and gate stack. All dimensions (L_g, $L_S/_D$, W_n, H_n, t_{ox}) require atomic-scale (±0.2 nm) control at sub-3 nm nodes.

Transconductance (g_m) and Gate Control:

Transconductance ($g_m = \partial I_D/\partial V_G$) quantifies the gate's ability to modulate channel charge. Thanks to their gate-all-around structure,

GAAFETs achieve stronger gate-channel coupling capacitance and reduced charge sharing, resulting in significantly higher g_m than FinFETs at equivalent dimensions.[16] With the gate enveloping the channel from all sides, even small variations in gate voltage induce greater charge modulation. Higher g_m not only improves digital switching speed but also benefits analog and RF applications by delivering higher gain and bandwidth. Specifically, recent 3 nm GAAFET simulations using the GT3 open-source PDK indicate marked improvements in drive current and subthreshold swing compared to junctionless transistor designs, further confirming GAAFET's advantages at extreme scaling.[17,18] Complementing these findings, TCAD work at the projected 2 nm node shows that both lateral- and vertical-nanosheet GAAFETs maintain superior I_{on}/I_{off} and short-channel control over equivalent nanowire and FinFET geometries, even when effective widths are swept from 18 nm to 54 nm.[19]

Subthreshold Swing (SS) and Off-State Leakage (I_{off}):

Subthreshold swing (SS) reflects the steepness of the transition from off to on state and is defined as the gate voltage required to change the drain current by one order of magnitude. The ideal thermal limit is ~60 mV/dec at room temperature. FinFETs at advanced nodes typically exhibit SS values in the 70–80 mV/dec range due to partial leakage from the fin top. In contrast, GAAFETs approach the theoretical limit more closely due to complete channel encapsulation.[16] Practically, GAAFETs can reduce I_{off} by 30–50% compared to FinFETs at similar gate lengths and voltages.[20] This significant leakage reduction supports operation at lower threshold and supply voltages, contributing to lower static power consumption and improved energy efficiency.[21]

In Table 1, we summarize the adoption timelines and reported performance/power improvements of FinFET and GAAFET technologies across leading manufacturers, illustrating how GAAFETs deliver superior electrostatics and power scaling at the 5 nm, 3 nm, and upcoming 2 nm nodes.

Table 1. Comparison of FinFET and GAAFET adoption across leading semiconductor manufacturers.

Company	Technology	Transistor Architecture	Performance & Power Gains	Production Timeline
TSMC	N3 (3 nm)	FinFET	+10–15% performance, -25–30% power (vs. 5 nm)	2022 - 2023
Samsung	3 nm	GAAFET (MBCFET™)	-45% power, +23% performance, -16% area (vs. 5 nm)	Early production in 2022, high volume in 2024
Intel	20A (~2 nm)	GAAFET (RibbonFET)	Expected benefits of nanosheet stacking	2024 (production), 2025 (commercial launch)
IBM	2 nm (prototype)	GAAFET (Nanosheet FET)	+45% performance, -75% power (vs. 7 nm)	2021 (research phase)

Drain-Induced Barrier Lowering (DIBL) and Short-Channel Effects:

DIBL measures the reduction in threshold voltage as the drain voltage increases – a critical indicator of short-channel control. GAAFETs, with their fully surrounding gate, exhibit superior electrostatic confinement, thereby minimizing the influence of drain electric fields. Consequently, GAAFETs achieve substantially lower DIBL than FinFETs at the same channel length.[16,22] Lower DIBL ensures robust device operation at reduced supply voltages and mitigates premature conduction due to drain bias, which is crucial for ultra-low-power designs. In contrast, FinFETs exhibit worsening SS and DIBL performance as channel lengths shrink near 5 nm.[6]

Table 1 summarizes key performance

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parameters, demonstrating that GAAFETs outperform FinFETs in terms of I_{on}, g_m, SS, and DIBL at equivalent technology nodes. These improvements stem directly from the gate-all-around architecture, establishing GAAFETs as the preferred option for 5 nm, 3 nm, and beyond.

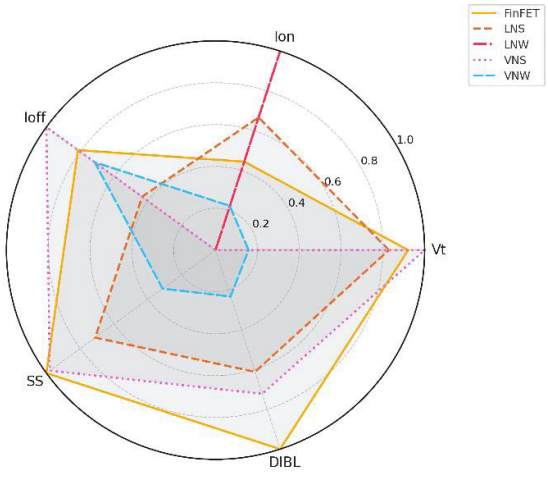

Figure 3. Radar chart comparing normalized performance metrics of FinFET and various GAAFET configurations at the 3 nm node: long nanosheet (LNS), long nanowire (LNW), vertical nanosheet (VNS), and vertical nanowire (VNW). Metrics include threshold voltage (V_t), on-current (I_{on}), off-current (I_{off}), subthreshold swing (SS), and DIBL, each scaled between 0 (worst) and 1 (best) for fair comparison.[19]

2.2. Leakage reduction and power efficiency

As technology nodes scale down, leakage current becomes a dominant factor in overall power consumption. FinFETs reduced leakage relative to planar FETs by introducing tri-gate control, but the top of the fin remains partially exposed. At nanoscale dimensions, this exposes the channel to fringe fields that can induce parasitic conduction - even when the device is off.[23] Figure 3 highlights the comparative plot of Ion, SS, and DIBL for FinFET vs. GAAFET.

GAAFETs address this by fully enclosing the channel. With gate coverage on all sides, electrostatic control becomes more uniform, eliminating weak leakage paths. Experimental results at 3-5 nm nodes show that GAAFETs can reduce subthreshold leakage (I_{off}) by approximately 30-50% compared to FinFETs under equivalent bias and geometry conditions.[16,20] This translates to significantly lower standby power in digital systems and improved energy efficiency, especially in battery-powered and ultra-low-power applications.

Moreover, better subthreshold slope and reduced DIBL in GAAFETs enable lower threshold voltages and supply voltages without sacrificing switching behavior. Since dynamic power scales with CV^2f, the ability to lower V_{dd} while maintaining performance directly improves energy efficiency. For instance, Samsung's migration to GAAFETs at 3 nm allowed operation at reduced V_{dd}, yielding up to 45% total power reduction.[13]

In summary, GAAFETs offer substantial improvements in leakage control, enabling lower-voltage operation and reduced active and standby power. The ability to continuously scale nanosheet width further enhances efficiency and tuning capability compared to the quantized nature of FinFET fins. These attributes make GAAFETs especially well-suited for next-generation low-power and high-density logic circuits.[21]

2.3. Design flexibility and integration considerations

A frequently underappreciated advantage of GAAFETs lies in their design scalability. In FinFET-based standard cell libraries, drive strength is quantized by the number of fins per transistor. For example, scaling from a 2-fin to a 3-fin inverter results in a 50% width increase and a proportional jump in capacitance. This granularity can complicate timing and power

optimization,[10] and necessitates creating and validating multiple variants (so-called FinFET binning), increasing design and verification overhead.

In contrast, GAAFETs provide continuous sizing flexibility. Designers can adjust the width of each nanosheet or the number of sheets lithographically to achieve the desired drive strength.[11] This allows library cells to be defined in finer width increments, reducing the number of distinct cells and enabling more precise timing/power trade-offs. For example, a designer could target a transistor width equivalent to 2.4 fins rather than being constrained to discrete integers. This granularity supports improved power distribution and timing closure in VLSI implementation.

From an integration standpoint, however, GAAFETs introduce new challenges. Their 3D stacked architecture requires careful routing and contact placement. Design rules may impose constraints on device placement to maintain nanosheet alignment or gate pattern uniformity. Furthermore, process modifications such as the use of SiGe for nanosheet release, or novel spacer and dielectric materials, must be co-optimized with physical design rules to ensure manufacturability and yield.

GAAFETs deliver superior device performance, better power efficiency, and enhanced design scalability compared to FinFETs. While their fabrication demands more complex integration efforts, their benefits are substantial enough to justify the industry-wide shift to GAAFETs at the 3 nm node and beyond. Table 3 provides a qualitative overview of technology readiness: FinFETs remain viable at 7 nm and 5 nm, but beyond this, GAAFETs offer a clear advantage in sustaining Moore's Law through improved electrostatics, power scaling, and layout flexibility.

Table 2. Estimated cost and yield comparison between FinFET and GAAFET platforms at the 3 nm node.

Metric	FinFET (N3)	GAAFET (SF3E/20A)
Mask Count	78	88
High-NA EUV usage	No	Partial
Yield (first year)	70%	55%
Cost per cm^2	$18.2	$23.7
Cost per logic gate	0.85 p$	1.12 p$

2.4. Cost-benefit analysis for commercial implementation

While GAAFETs promise better electrostatic control and scaling, their manufacturing complexity leads to trade-offs in cost and yield. Das et al.[8] report that MBCFET/GAAFET integration typically requires more photomasks than FinFET - roughly 88 vs. 78 masks at a given node - implying higher capital expenses. Scognamiglio et al[18] additionally confirm that process steps for advanced fin/stack alignment further increase fabrication time. Although detailed cost figures vary by foundry, the consensus is that initial GAAFET yield (~55 %) lags behind FinFET (~70 %) as reported by Ma et al.[24] Nevertheless, long-term gains in power efficiency and logic density - particularly when leveraging stress-engineered Si/SiGe channels[24] - may offset these upfront costs within one or two technology generations. Table 2 compares key metrics between FinFET and GAAFET technologies, including mask count, EUV exposure steps, and yield rates.

3.3. NM AND 2 NM NODE DEPLOYMENTS BY INDUSTRY LEADERS

To contextualize the FinFET versus GAAFET transition, we examine the strategies adopted by leading foundries at the 3 nm and 2 nm technology nodes. Table 3 compares the architectural choices of TSMC, Samsung, Intel, and IBM, alongside reported improvements in performance, power, and area. Figure 4 illustrates scaling trends in technology nodes and device density. Figure 5

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shows the claimed power reduction at the 3 nm and 2 nm nodes by major manufacturers.

Table 3. Comparison of 3 nm-class technology strategies by company.

Company	Node / Year	Transistor Architecture	Reported Gains (vs previous node)	Status (Year)
TSMC	N3 (~3 nm), 2022 - 23	FinFET (optimized)	+10–15% perf or -25–30% power vs N5 [16]	Mass production (2023)
Samsung	3 nm (SF3), 2022 - 24	GAAFET (Nanosheet, MBCFET™)	-45% power, +23% perf, -16% area vs 5 nm [11]	Initial prod. (2022), volume by 2024
Intel	20A (~2 nm), 2024	GAAFET (RibbonFET)	~+15% energy efficiency vs Intel 4 [19]	Risk production (2024), products ~2025
IBM	2 nm (research), 2021	GAAFET (Nanosheet)	+45% perf or -75% power vs 7 nm	Demo prototype (2021)

TSMC N3 (~3 nm, 2022-2023):

TSMC chose to retain FinFETs for its first-generation 3 nm node, branded as N3. By extensively optimizing fin dimensions and fabrication processes, TSMC achieved a reported 10 - 15% improvement in performance at iso-power, or a 25 - 30% reduction in power at iso-performance, relative to its 5 nm (N5) process.[21] The decision to stay with FinFETs was driven by the ability to meet performance targets without altering the device architecture, thereby leveraging the existing FinFET manufacturing infrastructure and mitigating risks associated with adopting a new device type. However, N3 is widely expected to be TSMC's final FinFET node for high-performance logic. According to the company's roadmap, it plans to transition to nanosheet-based transistors at the 2 nm generation (referred to as N2), with a projected rollout around 2025.

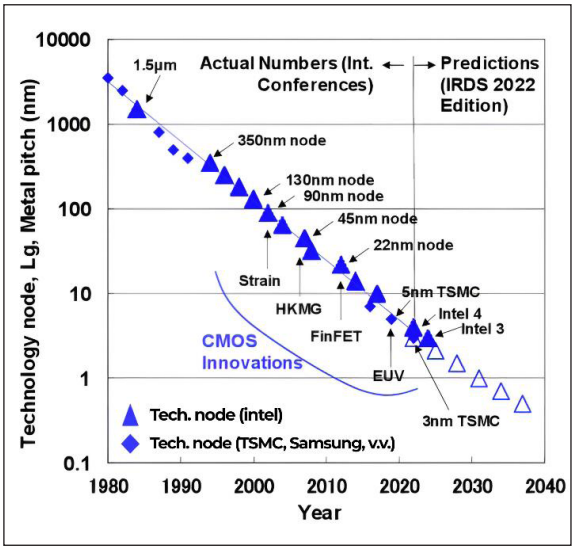

Figure 4. CMOS node shrink from 1.5 µm (1980) to 3 nm (2022) with IRDS-2022 projections toward sub-2 nm. Filled symbols show reported nodes (▲ Intel, ◆ TSMC/Samsung/others); open symbols △ mark IRDS forecasts. Key milestones-strain, HKMG, FinFET, EUV, and GAAFET-are annotated on the log-scale plot of gate length/metal pitch versus year.

Samsung 3 nm (2022 pilot, 2024 volume):

Samsung adopted a more aggressive strategy, becoming the first company in the industry to introduce a GAAFET-based technology into commercial production. At the 3 nm node, Samsung deployed its Multi-Bridge Channel FET (MBCFET™) architecture, based on horizontally stacked silicon nanosheets. Initial chip production on the 3 nm GAA process began in 2022. The company reported substantial improvements over its 5 nm FinFET process, including up to a 45% reduction in power consumption, 23% performance gain, and 16% area reduction.[13] These gains stem from both architectural advancements and process improvements. By 2024, Samsung aims to scale this technology for high-volume manufacturing and is concurrently developing a second-generation 3 nm GAAFET with anticipated performance gains of up to 30% and power savings of 50% relative to 5 nm. Samsung's early adoption has allowed it to gain a first-mover advantage in refining GAA

processes, though initial challenges such as yield optimization and ecosystem maturity remain.

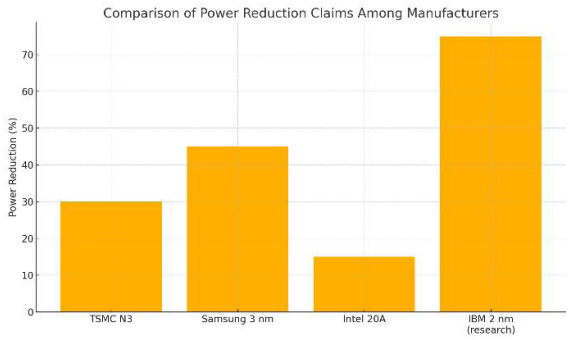

Figure 5. Claimed power reduction for 3 nm and 2 nm nodes by major manufacturers (TSMC, Samsung, Intel, IBM).

Intel 20A (~2 nm, 2024):

Intel plan to introduce its RibbonFET architecture - a proprietary implementation of nanosheet GAAFETs - at the "20A" node (20 Ångströms, approximately equivalent to 2 nm). RibbonFET will be paired with Intel's backside power delivery network technology, PowerVia.[26] According to Intel, RibbonFET is expected to deliver a 15% improvement in energy efficiency compared to Intel 4, either through higher performance at the same power or lower power at the same performance level.[27] The architecture involves stacking multiple horizontal nanoribbons for both PMOS and NMOS transistors and is central to Intel's goal of regaining leadership in process performance. Intel's 20A timeline aligns with TSMC's N2 roadmap, with early risk production reported in 2024 and commercial product release targeted for 2025. Intel's adoption of GAAFET technology reinforces the growing consensus that gate-all-around transistors are essential at the 2 nm node and beyond.[28]

IBM 2 nm GAAFET Prototype (2021):

In 2021, IBM - working in collaboration with research partners - demonstrated a 2 nm test chip fabricated using nanosheet GAAFETs.[29] The prototype contained 50 billion transistors on a compact chip footprint and showcased significant performance and efficiency potential: up to 45% performance improvement or 75% power savings relative to a 7 nm baseline.[30] While not intended for commercial deployment, the demonstration used a 300 mm wafer fabrication platform and featured gate lengths in the 12-14 nm range with vertically stacked nanosheets. IBM's prototype served as a key proof-of-concept for the feasibility of nanosheet transistors at extremely scaled dimensions, boosting industry confidence in GAAFET adoption.

TSMC's cautious, infrastructure-leveraged approach and Samsung's aggressive early GAAFET deployment highlight contrasting risk strategies. Intel's plan solidifies the view that GAAFETs are essential for scaling to 2 nm. IBM's research, though exploratory, helped validate the technical path that others are now commercializing. Beyond these four leaders, other foundries such as GlobalFoundries and SMIC are also investigating GAAFETs, though they remain behind in advanced node implementation.

Overall, the semiconductor industry has converged on a clear consensus: GAAFETs are the dominant transistor architecture for the 3 nm and 2 nm nodes. By the mid-2020s, all major vendors are expected to incorporate some form of gate-all-around architecture into their manufacturing processes.

4. POTENTIAL OF 2D MATERIALS FOR POST-3 NM TRANSISTOR SCALING

While silicon-based gate-all-around field-effect transistors (GAAFETs) are expected to sustain Moore's Law down to approximately 2 nm technology nodes, extending transistor scaling beyond this limit likely necessitates novel channel materials. Among the most promising candidates are two-dimensional (2D) materials - crystalline structures only a few atoms thick - which have garnered substantial attention as

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channels for sub-1 nm transistor technologies. Transition metal dichalcogenides (TMDs), such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), are the most extensively studied representatives of this material class. These materials naturally form layered monolayers ~0.7 nm thick, while retaining semiconducting properties, including appropriate bandgaps (~1.8 eV for monolayer MoS_2).

A key advantage of monolayer 2D semiconductors lies in their exceptional electrostatic control. Because the channel comprises a single atomic layer, the gate can modulate all carriers directly, eliminating deep-channel effects. This enables ultra-short gate lengths with strong suppression of short-channel effects. For instance, monolayer MoS_2 FETs have demonstrated operation at 1 nm gate lengths using carbon nanotube gates, with acceptable on/off current ratios – performance metrics unachievable with bulk silicon due to leakage currents at such scales.[14]

Another intrinsic benefit is the absence of surface dangling bonds. Both surfaces of a monolayer are naturally passivated, which facilitates atomically clean interfaces with gate dielectrics. In contrast to silicon, which requires careful thermal oxidation to minimize interface traps, 2D semiconductors can sustain steep subthreshold swings close to the thermionic limit (~60 mV/dec) even at short channel lengths.[31] High-performance MoS_2 transistors, for example, have demonstrated subthreshold swings around 70 mV/dec, and theoretical studies suggest that values below 60 mV/dec may be achievable using advanced gating methods.[32]

Although atomic in thickness, 2D materials exhibit moderate to high carrier mobilities. While silicon mobility declines rapidly at ultra-thin dimensions due to surface roughness and quantum confinement, monolayer MoS_2 devices have exhibited room-temperature electron mobilities of ~200 $cm^2/V{\cdot}s$ in short-channel configurations.[33] While this is lower than bulk silicon, the robustness of MoS_2 at the atomic scale is significant. Moreover, other 2D materials such as black phosphorus and heterostructured TMDs may offer even higher mobilities. Importantly, 2D semiconductors can often tolerate stronger electrostatic doping and gating fields, providing more flexibility for threshold voltage tuning.

Integration with Advanced Device Architectures

2D semiconductors are being explored not only for planar FETs but also in GAAFET configurations.[34] For example, researchers have implemented monolayer MoS_2 and WSe_2 within GAA structures, where the gate completely wraps around the 2D channel encapsulated by insulators. Recent demonstrations have achieved record-high drive currents ($I_{on} \approx 90$ μA/μm) and subthreshold swings as low as 85 mV/dec, even at extremely short gate lengths.[35] While these results still trail behind those of silicon-based GAAFETs, improvements are accelerating. Furthermore, the vertical stackability of 2D materials opens pathways toward monolithic 3D integration, including complementary FET (CFET) architectures - such as stacking a p-type WSe_2 FET atop an n-type MoS_2 FET.

Challenges for Scalable Manufacturing

Despite their promise, significant challenges must be overcome to integrate 2D materials into high-volume semiconductor manufacturing.

Wafer-Scale Synthesis:

Current approaches for producing high-quality 2D layers - such as mechanical exfoliation or small-scale chemical vapor deposition (CVD) - are inadequate for industrial adoption. For CMOS fabs, it is essential to develop processes capable of growing uniform monolayer films across 300 mm wafers. Techniques like metal-organic CVD (MOCVD) have shown promise for MoS_2 and WS_2, but achieving high monolayer uniformity (>99%)

and low defect densities (<10^8 cm^{-2}) remains a major challenge.[32] Advanced approaches such as seeded growth, phase-selective deposition, and surface functionalization are being investigated to meet these stringent requirements.[14]

Contact Resistance:

Forming low-resistance ohmic contacts to 2D semiconductors is particularly challenging due to the absence of out-of-plane bonds and Fermi level pinning, which lead to high Schottky barriers and contact resistances ranging from tens to hundreds of kΩ·μm.[14] One promising approach involves phase engineering, where the semiconducting 2H phase of MoS_2 is locally converted to a metallic 1T' phase, improving band alignment and reducing resistance.[31] Other strategies include edge-contact geometries, where electrodes contact the exposed edges of 2D sheets, and the insertion of interfacial layers such as graphene or metallic TMDs. Some configurations have achieved <1 kΩ·μm contact resistance, though further innovation is required to match silicon's performance (~10-50 Ω·μm).[34,35]

Dielectric Integration and Thermal Stability:

2D semiconductors must be compatible with high-κ gate dielectrics like HfO_2 and withstand backend-of-line (BEOL) thermal budgets (~400 °C). Although their dangling-bond-free surfaces enable low interface trap densities, defects can form during dielectric deposition, especially with plasma-assisted atomic layer deposition (ALD). Researchers are exploring gentler deposition methods, including surface pre-functionalization to initiate uniform nucleation without channel damage. Ensuring long-term stability in mobility and threshold voltage under thermal and electrical stress remains a critical area of investigation.[31]

2D semiconductors represent a compelling solution for extending transistor scaling into the angstrom regime, potentially mitigating the electrostatic and physical limitations of bulk silicon. While integration into mainstream CMOS requires substantial advances in materials science, device engineering, and process technology, progress is steady. Each year brings improvements in device performance metrics -including current drive, subthreshold swing, and contact resistance – as well as better methods for large-area monolayer synthesis. Within the next 5-10 years, it is plausible that 2D FETs may be deployed in niche low-power applications or 3D-stacked logic architectures. Section 5 will examine how these advances align with broader fabrication and system-level integration challenges.

5. FABRICATION CHALLENGES AND HETEROGENEOUS INTEGRATION STRATEGIES

As semiconductor scaling advances toward the 3 nm, 2 nm, and sub-2 nm nodes, fabrication challenges have become as significant as innovations in device architecture. This section highlights key manufacturing obstacles at these advanced nodes and explores heterogeneous integration strategies that complement traditional scaling.

EUV Lithography Limitations

The introduction of extreme ultraviolet (EUV) lithography at the ~7 nm node has enabled further miniaturization. However, despite operating at a 13.5 nm wavelength, EUV systems face fundamental resolution limits for features below 3 nm. While high-numerical-aperture (high-NA) EUV is expected to extend patterning capabilities, sub-3 nm features often still require multiple-patterning techniques to define nanosheets, fins, and tightly spaced interconnects.

Each additional patterning step increases complexity, variability, and cost. Moreover, stochastic effects inherent to EUV-such as photon shot noise and resist bridging-introduce random defects at the nanometer scale. As a result, the industry is investing in resist development, anti-

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collapse formulations, and restrictive design rules to maintain pattern fidelity. The deployment of EUV and multi-patterning technologies has also led to a sharp rise in wafer costs, making the economic feasibility of advanced nodes a critical concern.

Process Variability and Control

At these dimensions, atomic-scale control is essential. In gate-all-around FETs (GAAFETs), variations in nanosheet or gate dielectric thickness across the wafer-on the order of fractions of a nanometer-can cause substantial shifts in threshold voltage and leakage current. Ma et al[24] specifically identified that even minor variations in source/drain height substantially affect device characteristics, underscoring the critical need for rigorous atomic-scale process control at sub-3 nm nodes. Additionally, Zhu et al.[25] have shown that stress-induced mobility enhancement through Si/SiGe hybrid-channel integration can yield substantial performance gains, further highlighting strain engineering as crucial for sub-3 nm transistor optimisation. To meet these tolerances, advanced process techniques such as atomic layer deposition (ALD) and atomic layer etching (ALE) are employed.

Equally critical is metrology: in-line measurement of sub-nanometer features is non-trivial. Tools like spectroscopic ellipsometry, CD-SEM, and cross-sectional TEM are often used, but typically limited to test structures. Furthermore, classical ion implantation is being replaced due to variability at small scales. Instead, threshold tuning is achieved via in-situ doped epitaxial source/drain regions or through work-function modulation of gate metals.

Thermal and Power Density Constraints

Even though individual transistors become more energy-efficient, increasing transistor density drives up overall power density. Thermal management becomes more challenging as billions of transistors are densely integrated on a single die. Power delivery architecture is critical to mitigating thermal hotspots and IR drop.

Intel's PowerVia architecture exemplifies innovation in this area. By delivering power from the backside of the wafer in conjunction with RibbonFET technology, PowerVia improves IR drop, reduces front-side routing congestion, and enhances thermal uniformity. Nevertheless, design constraints such as "dark silicon" - where not all transistors can be activated simultaneously due to thermal limitations - remain a concern.

Cost and Yield Considerations

Historically, cost per transistor declined with each successive node. However, at 5 nm and beyond, this trend has slowed or even reversed.[15] EUV lithography, increased process complexity, and reduced yield have significantly raised wafer costs, particularly at 3 nm. These cost pressures are driving a paradigm shift toward chiplet-based architectures.

Rather than producing a single monolithic die at the latest node, designers can partition functionality into smaller chiplets. Critical logic blocks can be fabricated at 3 nm, while less performance-sensitive blocks such as I/O and analog functions are implemented on mature nodes like 14 nm. These chiplets are then integrated via advanced packaging techniques, optimizing overall performance, yield, and cost.[13]

3D Heterogeneous Integration and Emerging Architectures

Beyond 2.5D chiplet integration, three-dimensional (3D) stacking is emerging as a key strategy for density scaling. Through-silicon vias (TSVs) and wafer-to-wafer bonding enable vertical stacking of dies, such as memory-on-logic or logic-on-logic configurations.

Of particular interest is the Complementary FET (CFET) architecture, where NMOS and PMOS transistors are stacked vertically rather than placed laterally.[23] This configuration doubles

effective transistor density while maintaining CMOS functionality. CFETs can be realized by vertically stacking two GAAFETs using either silicon nanosheets or 2D materials. While early demonstrations confirm CFET feasibility, precise alignment and vertical interconnect formation remain formidable challenges.

Another novel approach is the Vertical Transport FET (VTFET), pioneered by IBM and others. In VTFETs, the current flows vertically from source to drain, and the gate wraps around a vertical channel. This configuration offers over 2× density improvements compared to planar transistors, with potential performance gains.[17]

Both CFET and VTFET architectures are still in the research and development phase but are being actively explored as potential successors to GAAFETs when lateral scaling saturates.

Design-Technology Co-Optimization (DTCO) and System-Level Gains

The increasing complexity of advanced nodes necessitates design-technology co-optimization (DTCO). Designers must understand manufacturing constraints, while process engineers must provide levers (e.g., new devices, layout options) that designers can exploit. DTCO is critical to extracting maximum value from each technology generation.

Heterogeneous integration is increasingly viewed as the third pillar of progress, alongside device scaling and circuit-level innovation. System-level benefits such as reduced memory access latency and lower energy per operation can be achieved by vertically stacking memory and logic. Similarly, chiplet designs enable function-specific optimization across different process nodes, improving both performance-per-watt and performance-per-dollar.

Scaling to 3 nm and beyond is no longer just a matter of shrinking transistors. It requires multidisciplinary innovation across materials science (e.g., novel channels and dielectrics), electrical engineering (e.g., CFETs, VTFETs), and computer architecture (e.g., chiplet systems, DTCO). Heterogeneous integration is now a cornerstone strategy for sustaining Moore's Law—allowing meaningful system-level advancements even when traditional transistor scaling slows. The next section will explore the broader implications of these developments on the future of semiconductor technology.

6. CONCLUSION AND OUTLOOK

Transistor scaling has reached a stage where geometric and material innovations are as essential as dimensional reduction. Gate-All-Around FETs (GAAFETs), notably nanosheet transistors, have demonstrated their viability at the 3 nm node, delivering improved performance and energy efficiency. This analysis confirms that GAAFETs outperform FinFETs in drive current, electrostatic control, and leakage, validating the industry's shift to GAAFETs for 3 nm and 2 nm technologies. Early deployments by Samsung and Intel further affirm GAAFETs as practical solutions for next-generation CMOS.

Looking ahead, several critical directions are emerging:

• *New Materials for Scaled Channels:* Two-dimensional (2D) semiconductors offer compelling properties—atomic-scale thickness, strong gate control, and reduced short-channel effects—that make them prime candidates for sub-2 nm technologies. Hybrid stacks, such as CFETs combining a silicon GAAFET and a 2D FET, may become a key architecture. High-mobility III–V compounds and strain-engineered SiGe are also under exploration for performance-critical applications like RF or analog blocks.

• *Beyond-GAAFET Device Architectures:* Vertical Transport FETs (VTFETs) and Complementary FETs (CFETs) extend scaling into the third dimension. VTFETs rotate the transistor vertically to improve density; CFETs vertically stack NMOS and PMOS to halve area. Lab demonstrations show promise 17,

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but challenges in manufacturability and circuit reliability remain. These devices could succeed GAAFETs later this decade.

• H*eterogeneous Integration and System Co-design:* As transistor pitch scaling slows, progress continues through packaging and architectural co-design—the essence of "More-than-Moore." Future systems will leverage 2.5D and 3D integration, combining chiplets across nodes and technologies (logic, memory, photonics) within a single package. Success demands cross-disciplinary collaboration spanning materials, devices, circuits, and systems.

In summary, the sub-3 nm roadmap presents formidable challenges, but also vast potential. GAAFETs have opened a path forward for near-term scaling, while emerging materials and 3D device architectures promise long-term extension. Realizing this future will require synergy between device physics, fabrication technology, and system design. With continued collaboration between academia and industry, the momentum of Moore's Law can be sustained-powering breakthroughs in computing, communications, and beyond.

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