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# Graphene transistors

Frank Schwierz[1]*

**Graphene has changed from being the exclusive domain of condensed-matter physicists to being explored by those in the electron-device community. In particular, graphene-based transistors have developed rapidly and are now considered an option for post-silicon electronics. However, many details about the potential performance of graphene transistors in real applications remain unclear. Here I review the properties of graphene that are relevant to electron devices, discuss the trade-offs among these properties and examine their effects on the performance of graphene transistors in both logic and radiofrequency applications. I conclude that the excellent mobility of graphene may not, as is often assumed, be its most compelling feature from a device perspective. Rather, it may be the possibility of making devices with channels that are extremely thin that will allow graphene field-effect transistors to be scaled to shorter channel lengths and higher speeds without encountering the adverse short-channel effects that restrict the performance of existing devices. Outstanding challenges for graphene transistors include opening a sizeable and well-defined bandgap in graphene, making large-area graphene transistors that operate in the current-saturation regime and fabricating graphene nanoribbons with well-defined widths and clean edges.**

Every now and again, a single paper ignites a revolution in science and technology. Such a revolution was started in October 2004, when condensed-matter physicists reported that they had prepared graphene—two-dimensional sheets of carbon atoms—and observed the electric field effect in their samples[1]. It was not long before this new material attracted the attention of the electron-device community, and today a growing number of groups are successfully fabricating graphene transistors. Major chip-makers are now active in graphene research and the International Technology Roadmap for Semiconductors, the strategic planning document for the semiconductor industry, considers graphene to be among the candidate materials for post-silicon electronics[2].

Several excellent reviews on the basic science of graphene have been published in recent years[3–5]. Given the growing interest in graphene in the electron-device community, and ongoing discussions of the potential of graphene transistors, a review article focusing on graphene devices is timely. Here, from the point of view of a device engineer, I discuss the potential of graphene as a new material for electron devices, and summarize the state of the art for graphene transistors. I will focus mostly on the field-effect transistor (FET), because this is the most successful device concept in electronics and because most work on graphene devices so far has been related to FETs.

Two principal divisions of semiconductor electronics are digital logic devices and radiofrequency devices. The degree of readiness to introduce new device concepts is generally higher for radiofrequency applications, in part because the fortunes of digital logic depend almost entirely on the performance of a single type of device: the silicon metal–oxide–semiconductor FET (MOSFET). For decades, making MOSFETs smaller has been key to the progress in digital logic. This size scaling has enabled the complexity of integrated circuits to double every 18 months, leading to significant improvements in performance and decreases in price per transistor[6,7]. Today, processors containing two billion MOSFETs, many with gate lengths of just 30 nm, are in mass production (Fig. 1).

Because the fabrication of integrated circuits is highly complex, semiconductor fabrication plants are extremely expensive (at present costing several billion US dollars). Furthermore, because scaling alone has provided the needed performance improvements from one generation of integrated circuits to the next, there has been little motivation for the chip-makers to introduce devices based on a fundamentally different physics or on a material other than silicon. However, there is a consensus in the community that MOSFET scaling is approaching its limits and that, in the long run, it will be necessary to introduce new material and device concepts to ensure that performance continues to improve.

The situation is different for radiofrequency electronics. This field was dominated by defence applications until the late 1980s, and although it moved into the mainstream in the 1990s owing to advances in wireless communications, the military continued to provide generous financial support for research into new radiofrequency devices. This, together with the fact that radiofrequency circuits are much less complex than digital logic chips, has led to makers of radiofrequency chips being more open to new device concepts. An indication of this is the large variety of different transistor types and materials used in radiofrequency electronics: these include high-electron-mobility transistors (HEMTs) based on III–V semiconductors such as GaAs and InP, silicon n-channel MOSFETs, and different types of bipolar transistor[8,9].

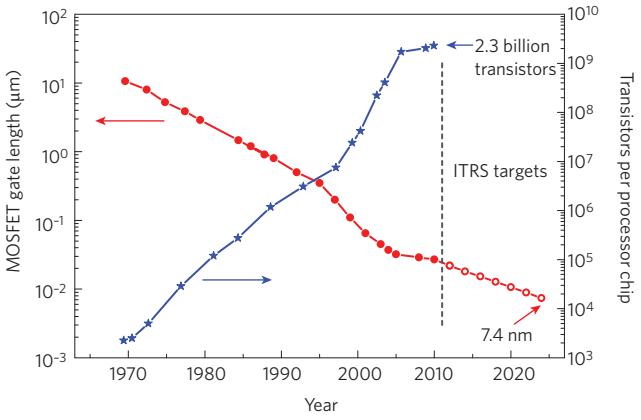


**Figure 1 | Trends in digital electronics.** Evolution of MOSFET gate length in production-stage integrated circuits (filled red circles) and International Technology Roadmap for Semiconductors (ITRS) targets (open red circles). As gate lengths have decreased, the number of transistors per processor chip has increased (blue stars). Maintaining these trends is a significant challenge for the semiconductor industry, which is why new materials such as graphene are being investigated.

[1]Technische Universität Ilmenau, Postfach 100565, 98694 Ilmenau, Germany. *e-mail: frank.schwierz@tu-ilmenau.de

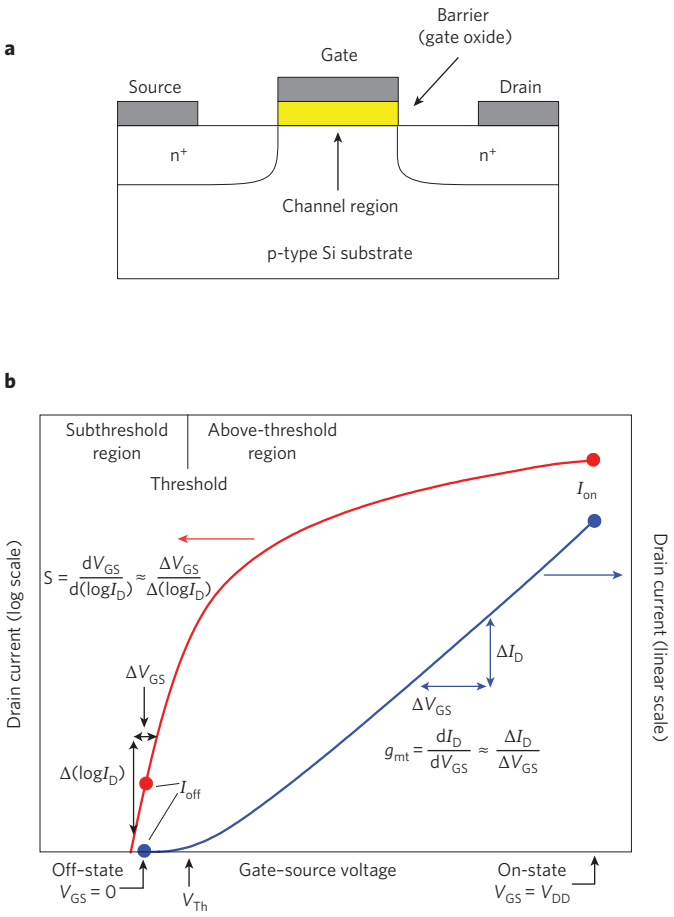


**Figure 2 | Conventional FETs. a**, Cross-section of an n-channel Si MOSFET. When the voltage applied between the source and gate electrodes exceeds a threshold voltage, $V_{Th}$, a conducting channel is formed and a drain current, $I_D$, flows. The length of the channel is defined by the length of the gate electrode; the thickness of the gate-controlled channel region is the depth to which the electronic properties of the semiconductor (p-doped Si in this case) are influenced by the gate. **b**, FET transfer characteristics showing $I_D$ (on a logarithmic scale on the left and a linear scale on the right) versus the gate–source voltage, $V_{GS}$. The transistor is considered to be switched on when $V_{GS}$ is equal to the maximum voltage supplied to the device, $V_{DD}$. The higher the slope in the subthreshold region ($V_{GS} < V_{Th}$), the better the transistor switch-on characteristics become. Above threshold, the change in $I_D$ for a given change in $V_{GS}$ is called the terminal transconductance, $g_{mt}$.

As I discuss below, graphene is potentially well suited to radiofrequency applications because of its promising carrier transport properties and its purely two-dimensional structure. This, combined with the relative openness of the radiofrequency-electronics industry to new materials, suggests that graphene might make its first appearance in radiofrequency applications rather than in logic circuits.

## FET physics: what really matters

A FET consists of a gate, a channel region connecting source and drain electrodes, and a barrier separating the gate from the channel (Fig. 2a). The operation of a conventional FET relies on the control of the channel conductivity, and thus the drain current, by a voltage, $V_{GS}$, applied between the gate and source.

For high-speed applications, FETs should respond quickly to variations in $V_{GS}$; this requires short gates and fast carriers in the channel. Unfortunately, FETs with short gates frequently suffer from degraded electrostatics and other problems (collectively known as short-channel effects), such as threshold-voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation[7,10]. Scaling theory predicts that a FET with a thin barrier and a thin gate-controlled region (measured in the vertical direction in Fig. 2a) will be robust against short-channel effects down to very short gate lengths (measured in the horizontal direction in Fig. 2a)[11]. The possibility of having channels that are just one atomic layer thick is perhaps the most attractive feature of graphene for use in transistors. (Mobility, which is often considered to be graphene's most useful property for applications in nanoelectronics, is discussed later.) By comparison, the channels in III–V HEMTs are typically 10–15 nm thick, and although silicon-on-insulator MOSFETs with channel (that is, silicon body) thicknesses of less than 2 nm have been reported[12], rough interfaces caused their mobility to deteriorate. More importantly, the body of these MOSFETs showed thickness fluctuations that will lead to unacceptably large threshold-voltage variations (and similar problems are expected to occur when the thickness of the channel in a III–V HEMT is reduced to only a few nanometres). These problems occur at thicknesses that are many times greater than the thickness of graphene.

The series resistances between the channel and the source and drain terminals are also important, and their adverse impact on the FET becomes more pronounced as the gate length decreases[13]. Thus, device engineers devote considerable effort to developing transistor designs in which short-channel effects are suppressed and series resistances are minimized.

Modern digital logic is based on silicon complementary metal oxide semiconductor (CMOS) technology. CMOS logic gates consist of both n- and p-channel MOSFETs that can switch between the on-state (with a large on-current, $I_{on}$, and $V_{GS} = \pm V_{DD}$, where $V_{DD}$ is the maximum voltage supplied to the device) and the off-state (with a small off-current, $I_{off}$, and $V_{GS} = 0$). In the terminology of digital logic, a gate is not the gate terminal of a transistor but a combination of two or more transistors that can perform a certain logic operation. The value of $V_{GS}$ at which the FET is just on the verge of switching on is the threshold voltage, $V_{Th}$. Figure 2b shows the transfer characteristics of an n-channel FET indicating the on-state and the off-state. Useful measures with which to assess the switching behaviour are the subthreshold swing, $S$ (relevant to the subthreshold region), and the terminal transconductance, $g_{mt}$ (relevant to the above-threshold region).

In the steady state, a certain number of the MOSFETs in a CMOS logic gate are always switched off so that no current—except the small $I_{off}$—flows through the gate[14]. The ability of silicon MOSFETs to switch off enables silicon CMOS to offer extremely low static power dissipation (which is the reason why silicon CMOS has bested all competing logic technologies). Thus, any successor to the silicon MOSFET that is to be used in CMOS-like logic must have excellent switching capabilities, as well as an on–off ratio, $I_{on}/I_{off}$, of between $10^4$ and $10^7$ (ref. 2). In a conventional FET, this requires semiconducting channels with a sizeable bandgap, preferably 0.4 eV or more. Moreover, n- and p-channel FETs with symmetrical threshold voltages, that is, with $V_{Th,n} = -V_{Th,p}$, are needed for proper CMOS operation.

In radiofrequency applications, however, switch-off is not required *per se*. In small-signal amplifiers, for example, the transistor is operated in the on-state and small radiofrequency signals that are to be amplified are superimposed onto the d.c. gate–source voltage. To discuss the radiofrequency performance of FETs, I use the equivalent circuit from Fig. 3a and focus on the cut-off frequency, $f_T$, which is the frequency at which the magnitude of the small-signal current gain rolls off to unity. The cut-off frequency is the most widely used figure of merit for radiofrequency devices and is, in effect, the highest frequency at which a FET is useful in radiofrequency applications.

As can be seen from the expression for $f_T$ given in Table 1 (refs 7,8), the cut-off frequency can be maximized by making the intrinsic transconductance, $g_m$, as large as possible and making the

drain conductance, $g_{ds}$, and all the capacitances and resistances in the equivalent circuit (Fig. 3) as small as possible[7,8]. However, the values of all these quantities vary with the applied d.c. gate–source voltage, $V_{GS}$, and the applied d.c. drain–source voltage, $V_{DS}$. As shown exemplarily for a typical GaAs HEMT[15,16] (Fig. 3b,c), $V_{DS}$ has a pronounced effect on the FET performance. For this transistor, $f_T$ peaks around $V_{DS}$ = 1 V, that is, deep in the region of drain-current saturation, where $g_m$ is near its peak and $g_{ds}$ has decreased sufficiently. For lower values of $V_{DS}$, the device operates in the linear regime and the cut-off frequency is low because $g_m$ is small and $g_{ds}$ is large.

The bottom line for radiofrequency performance is that although shorter gates, faster carriers and lower series resistances all lead to higher cut-off frequencies, saturation of the drain current is essential to reach the maximum possible operating speeds. This point is frequently missed in discussions of transistor speeds. Drain-current saturation is also necessary to maximize the intrinsic gain, $G_{int} = g_m/g_{ds}$, which has become a popular figure of merit for mixed-signal circuits.

## Graphene properties relevant to transistors

Single-layer graphene is a purely two-dimensional material. Its lattice consists of regular hexagons with a carbon atom at each corner. The bond length between adjacent carbon atoms, $L_b$, is 1.42 Å and the lattice constant, $a$, is 2.46 Å (Fig. 4a). The first reports on this material appeared decades ago, even before the name graphene had been coined (see, for example, refs 17–19), but it took the pioneering 2004 paper by the Manchester group[1] to spark the present explosion of interest in the material.

At present, the most popular approaches to graphene preparation are mechanical exfoliation[1], growth on metals and subsequent graphene transfer to insulating substrates[20,21], and thermal decomposition of SiC to produce so-called epitaxial graphene on top of SiC wafers[22,23]. Exfoliation is still popular for laboratory use but it is not suited to the electronics industry, whereas the other two options both have the potential for producing wafer-scale graphene. After the graphene has been prepared, common semiconductor processing techniques (such as lithography, metallization and etching) can be applied to fabricate graphene transistors.

In this section, I discuss two important aspects of graphene: the presence (or otherwise) of a bandgap, and charge transport (mobility and high-field transport) at room temperature.

**Bandgap.** Large-area graphene is a semimetal with zero bandgap. Its valence and conduction bands are cone-shaped and meet at the K points of the Brillouin zone (Fig. 4b). Because the bandgap is zero, devices with channels made of large-area graphene cannot be switched off and therefore are not suitable for logic applications. However, the band structure of graphene can be modified, and it is possible to open a bandgap in three ways: by constraining large-area graphene in one dimension to form graphene nanoribbons, by biasing bilayer graphene and by applying strain to graphene. See Table 2 and refs 24–43 for more details.

It has been predicted[28] that both armchair nanoribbons and zigzag nanoribbons (the two ideal types of nanoribbon; Fig. 4a) have a bandgap that is, to a good approximation, inversely proportional to the width of the nanoribbon. The opening of a bandgap in nanoribbons has been verified experimentally for widths down to about 1 nm (refs 24–27), and theory and experiments both reveal bandgaps in excess of 200 meV for widths below 20 nm (Fig. 4c). However, it should be noted that real nanoribbons have rough edges and widths that change along their lengths. Even modest edge disorder obliterates any difference in the bandgap between nanoribbons with different edge geometries[29], and edge functionalization and doping can also affect the bandgap[44].

To open a bandgap useful for conventional field-effect devices, very narrow nanoribbons with well-defined edges are needed. This represents a serious challenge given the semiconductor processing

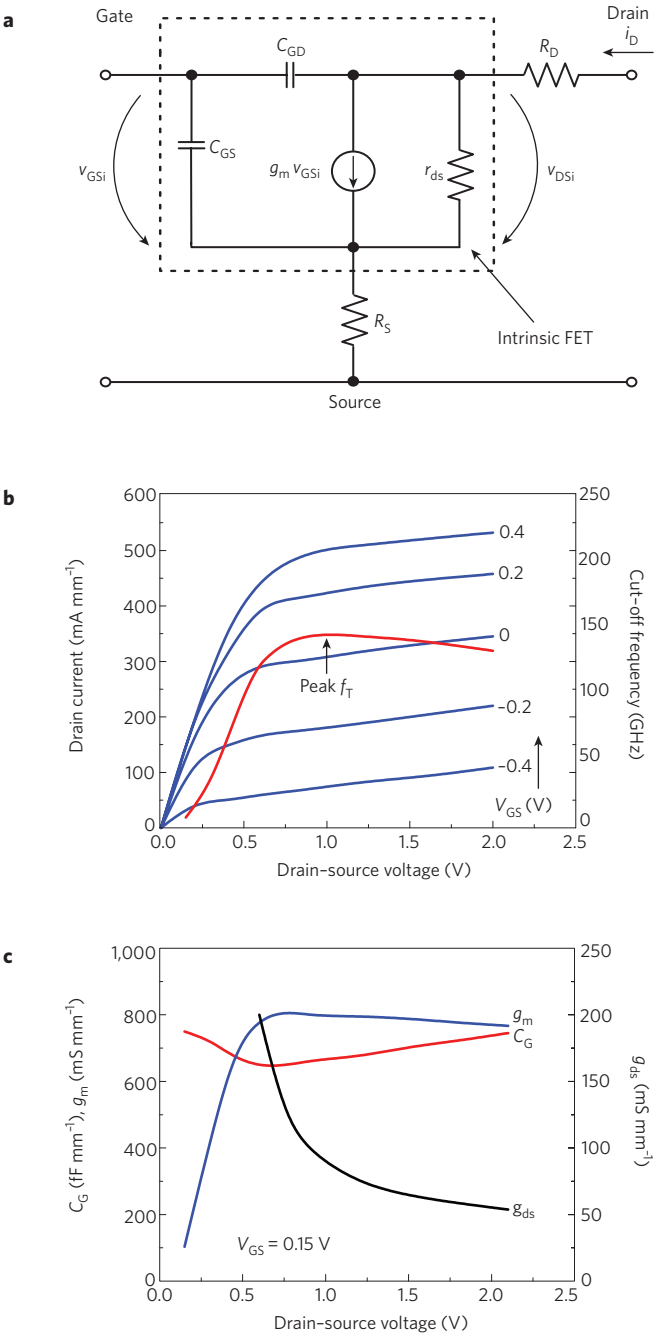


**Figure 3 | FET d.c. and small-signal operation. a**, Small-signal equivalent FET circuit. The intrinsic transconductance, $g_m$, is related to the internal small-signal gate–source and drain–source voltages, $v_{GSi}$ and $v_{DSi}$, whereas the terminal transconductance, $g_m$, is related to the applied gate–source and drain–source voltages, $V_{GS}$ and $V_{DS}$ (Table 1 and Fig. 2b). **b**, The drain current, $I_D$ (blue lines), at different values of $V_{GS}$, and the cut-off frequency, $f_T$ (red line), both versus $V_{DS}$ for a radiofrequency GaAs high-electron-mobility transistor[15,16]. The cut-off frequency peaks at $V_{DS}$ = 1 V and $V_{GS}$ = 0.15 V. **c**, The intrinsic transconductance (blue line), the overall gate capacitance, $C_G = C_{GS} + C_{GD}$ (red line), and the drain conductance, $g_{ds}$ ($1/r_{ds}$; black line), versus $V_{DS}$ for the same FET.

equipment available at the moment. Recently, nanoribbons that were uniform in width and had reduced edge roughness were produced by 'unzipping' carbon nanotubes[45]. However, even a perfect nanoribbon is not perfect for electronics applications. In general, the larger the bandgap that opens in a nanoribbon, the more the

**Table 1 | Performance measures for the field-effect transistor.**

| Quantity | Definition |
|---|---|
| Terminal transconductance | $g_{mt} = \left.\frac{dI_D}{dV_{GS}}\right\|_{V_{DS}=\text{const}}$ |
| Intrinsic transconductance | $g_m = \left.\frac{dI_D}{dV_{GSi}}\right\|_{V_{DSi}=\text{const}}$ |
| Drain conductance | $g_{ds} = \frac{1}{r_{ds}} = \left.\frac{dI_D}{dV_{DSi}}\right\|_{V_{GSi}=\text{const}}$ |
| Gate–source capacitance | $C_{GS} = -\left.\frac{dQ_{ch}}{dV_{GSi}}\right\|_{V_{DSi}=\text{const}}$ |
| Gate–drain capacitance | $C_{GD} = -\left.\frac{dQ_{ch}}{dV_{DSi}}\right\|_{V_{GSi}=\text{const}}$ |
| Cut-off frequency | $f_T \approx \frac{g_m}{2\pi} \frac{1}{(C_{GS}+C_{GD})[1+g_{ds}(R_S+R_D)]+C_{GD}g_m(R_S+R_D)}$ |
| Field-effect mobility | $\mu_{FE} = \frac{L_{ch}g_m}{W_{ch}C_G V_{DS}}$ |

$V_{GS}$, $V_{DS}$: terminal d.c. voltages; $V_{GSi}$, $V_{DSi}$: intrinsic d.c. voltages; $Q_{ch}$: mobile channel charge; $L_{ch}$, $W_{ch}$: channel length and width; $C_G$: gate capacitance. In the expression for $\mu_{FE}$, $C_G$ is the gate capacitance per unit area. $R_S$ and $R_D$ are the source and drain series resistances, respectively. Expressions for the terminal and intrinsic transconductances, drain conductance, gate–source and gate–drain capacitances, and cut-off frequency for the equivalent FET circuit shown in Fig. 3a[7,8]. The expression for the field-effect mobility in MOS channels is also shown[66].

valence and conduction bands become parabolic (rather than cone-shaped): this decreases the curvature around the K point and increases the effective mass of the charge carriers[46], which is likely to decrease the mobility.

Bilayer graphene is also gapless (Fig. 4b), and its valence and conduction bands have a parabolic shape near the K point. If an electric field is applied perpendicular to the bilayer, a bandgap opens and the bands near the K point take on the so-called Mexican-hat shape. This opening was predicted by theory[30,31] and has been verified in experiments[32,33]. Theoretical investigations have also shown that the size of the bandgap depends on the strength of the perpendicular field and can reach values of 200–250 meV for high fields ($(1–3) \times 10^7$ V cm$^{-1}$; refs 30,31).

The bandgap of large-area single-layer epitaxial graphene is at present the subject of controversy[34]. Although some results suggest a zero bandgap[37,38], others report a bandgap of around 0.25 eV (refs 35,36). The transfer characteristics of epitaxial-graphene MOSFETs show no switch-off, which suggests a zero bandgap. However, a bandgap is consistently observed for epitaxial bilayer graphene[38,39].

Finally, strain has been discussed as a means of opening a bandgap in large-area graphene, and the effect of uniaxial strain on the band structure has been simulated[40,41]. At present it seems that if it is possible at all, opening a gap in this way will require a global uniaxial strain exceeding 20%, which will be difficult to achieve in practice. Moreover, little is known about the ways in which other types of strain, such as biaxial strain and local strain, influence the band structure of graphene.

Thus, although there are a number of techniques for opening a bandgap in graphene, they are all at the moment some way from being suitable for use in real-world applications.

**Mobility.** The most frequently stated advantage of graphene is its high carrier mobility at room temperature. Mobilities of 10,000–15,000 cm$^2$ V$^{-1}$ s$^{-1}$ are routinely measured for exfoliated graphene on $SiO_2$-covered silicon wafers[1,47], and upper limits of between 40,000 and 70,000 cm$^2$ V$^{-1}$ s$^{-1}$ have been suggested[47,48]. Moreover, in the absence of charged impurities and ripples, mobilities of 200,000 cm$^2$ V$^{-1}$ s$^{-1}$ have been predicted[49], and a mobility of $10^6$ cm$^2$ V$^{-1}$ s$^{-1}$ was recently reported for suspended graphene[50]. For large-area graphene grown on nickel and transferred to a substrate, mobilities greater than 3,700 cm$^2$ V$^{-1}$ s$^{-1}$ have been measured[20].

Finally, for epitaxial graphene on silicon carbide, the mobility depends on whether the graphene is grown on the silicon face or the carbon face of SiC. Although graphene grown on the carbon face has higher mobility (values of ~5,000 cm$^2$ V$^{-1}$ s$^{-1}$ have been reported[23], compared with ~1,000 cm$^2$ V$^{-1}$ s$^{-1}$ for graphene grown on the silicon face[23,51]), it is easier to grow single-layer and bilayer graphene on the silicon face, which makes the silicon face of SiC more suited for electronic applications.

In early graphene MOS structures, the mobility was affected by the use of a top-gate dielectric[52,53]. However, the recent demonstration of mobilities of around 23,000 cm$^2$ V$^{-1}$ s$^{-1}$ in top-gated graphene MOS channels[54] and the observation of similar mobilities before and after top-gate formation[55] show that high-mobility graphene

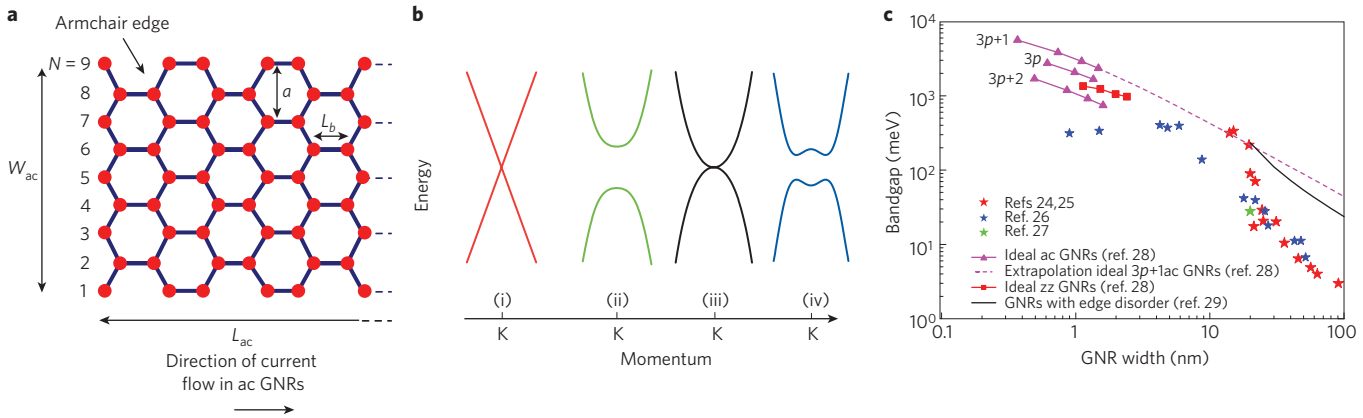


**Figure 4 | Properties of graphene and graphene nanoribbons. a**, Schematic of an armchair (ac) graphene nanoribbon (GNR) of length $L_{ac}$ and width $W_{ac}$. The nanoribbon shown here has $N = 9$ carbon atoms along its width and thus belongs to the 3*p* family, where *p* is an integer. **b**, Band structure around the K point of (i) large-area graphene, (ii) graphene nanoribbons, (iii) unbiased bilayer graphene, and (iv) bilayer graphene with an applied perpendicular field. Large-area graphene and unbiased bilayer graphene do not have a bandgap, which makes them less useful for digital electronics. **c**, Bandgap versus nanoribbon width from experiments[24–27] and calculations[28,29]. By comparison, the bandgap of Si is above 1 eV. zz: zigzag.

MOS channels can be made with a proper choice of the gate dielectric and optimization of the deposition process.

These mobility numbers are impressive, but they require closer inspection. The high mobilities mentioned above relate to large-area graphene, which is gapless. A general trend for conventional semiconductors is that the electron mobility decreases as the bandgap increases, and a similar trend has been predicted for carbon nanotubes (CNTs)[56,57] and graphene nanoribbons[58–61] (Fig. 5a). This means that the mobility in nanoribbons with a bandgap similar to that of silicon (1.1 eV) is expected to be lower than in bulk silicon and no higher than the mobility in the silicon channel of a conventional MOS device[58]. The mobilities measured in experiments—less than 200 $cm^2\ V^{-1}\ s^{-1}$ for nanoribbons 1–10 nm wide[26,62] and 1,500 $cm^2\ V^{-1}\ s^{-1}$ for a nanoribbon 14 nm wide[45] (which is the highest mobility so far measured for a nanoribbon)—support the theoretical results (Fig. 5b). Therefore, although the high mobilities offered by graphene can increase the speed of devices, they come at the expense of making it difficult to switch devices off, thus removing one of the main advantages of the CMOS configuration—its low static power consumption.

**High-field transport.** In the days when FETs had gates several micrometres long, the mobility was the appropriate measure of the speed of carrier transport. Strictly speaking, however, the mobility describes carrier transport in low electric fields; the short gate lengths in modern FETs result in high fields in a sizeable portion of the channel, reducing the relevance of mobility to device performance. To illustrate this, let us consider a FET with a gate 100 nm long and a drain–source voltage of 1 V. If we assume a voltage drop of 0.3 V across the series resistances, the average field in the channel is 70 kV $cm^{-1}$. At such high fields, the steady-state carrier velocity saturates, and this saturation velocity becomes another important measure of carrier transport. Figure 5c shows plots of the electron velocity versus the electric field for conventional semiconductors, and simulated plots for large-area graphene[63,64] and a carbon nanotube[57]. For graphene and the nanotube, maximum carrier velocities of around $4 \times 10^7$ cm $s^{-1}$ are predicted, in comparison with $2 \times 10^7$ cm $s^{-1}$ for GaAs and $10^7$ cm $s^{-1}$ for silicon. Moreover, at high fields the velocity in graphene and the nanotube does not drop as drastically as in the III–V semiconductors. Unfortunately, there is at present no experimental data available on high-field transport in graphene nanoribbons and in large-area graphene. However, other measurements[65] suggest high-field carrier velocities of several $10^7$ cm $s^{-1}$ in graphene. Thus, regarding high-field transport, graphene and nanotubes seem to have a slight advantage over conventional semiconductors.

Finally, it is worth noting that reported mobilities for graphene devices need to be interpreted carefully because there are several

**Table 2 | Does graphene have a bandgap?**

| Graphene type | Size | Bandgap | Remarks | Ref. |
|---|---|---|---|---|
| SL graphene on $SiO_2$ | LA | No | Experiment and theory | 1, 5 |
| SL graphene on $SiO_2$ | GNR | Yes | Experiment and theory; gap due to lateral confinement* | 24–29 |
| BL graphene on $SiO_2$ | LA | Yes | Experiment and theory; gap due to symmetry breaking by perpendicular interlayer field | 30–33 |
| Epitaxial SL | LA | Unknown | Controversial discussion | 34 |
| | | Yes | Experiment and theory, gap due to symmetry breaking | 35, 36 |
| | | No | Experiment and theory | 37, 38 |
| Epitaxial BL | LA | Yes | Experiment and theory | 32, 38, 39 |
| Epitaxial SL, BL | GNR | Yes | Theory | 39 |
| Strained SL† | LA | Yes | Theory; gap due to level crossing | 40 |
| | | No | Theory | 41 |

SL: single-layer; BL: bilayer; LA: large-area; GNR: graphene nanoribbon. *The origin of the bandgap in nanoribbons is still under debate: in addition to pure lateral confinement[28], it has been suggested that the Coulomb blockade[42,43] or Anderson localization[29] might be responsible for the formation of the gap. †Theorists disagree about the existence of a bandgap for strained SL graphene.

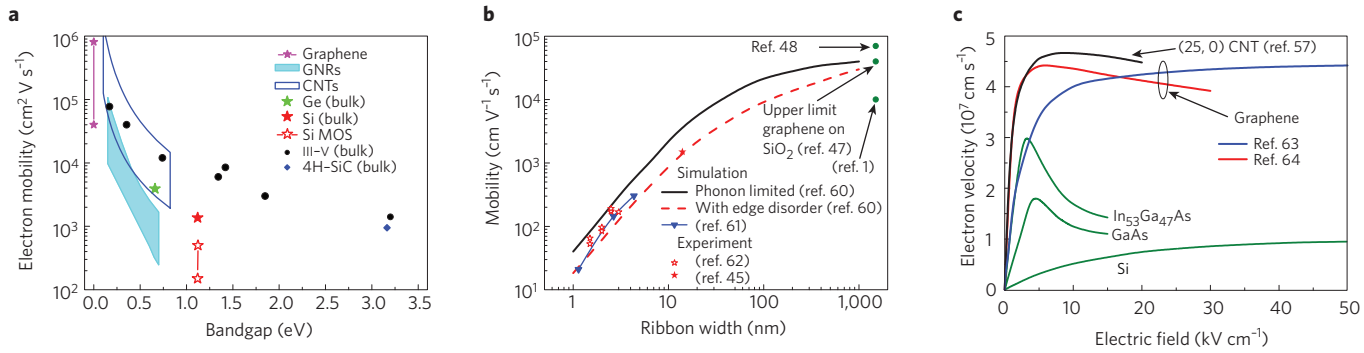


**Figure 5 | Carrier transport in graphene. a**, Electron mobility versus bandgap in low electric fields for different materials, as indicated (from left to right, III–V compounds are InSb, InAs, $In_{0.53}Ga_{0.47}As$, InP, GaAs, $In_{0.49}Ga_{0.51}P$, and GaN). The mobility data relates to undoped material except for the Si MOS data. Also shown are mobility data for carbon nanotubes (CNTs; simulation[56,57]), graphene nanoribbons (simulation[58,59]) and graphene (experiment and simulation[47–50]). **b**, Carrier mobility versus nanoribbon width at low electric fields from simulations[60,61] and experiments (open[62] and full[45] stars). Data for large-area graphene are also shown[1,47,48]. **c**, Electron drift velocity versus electric field for common semiconductors (Si, GaAs, $In_{0.53}Ga_{0.47}As$), a carbon nanotube (simulation[57]) and large-area graphene (simulation[63,64]).

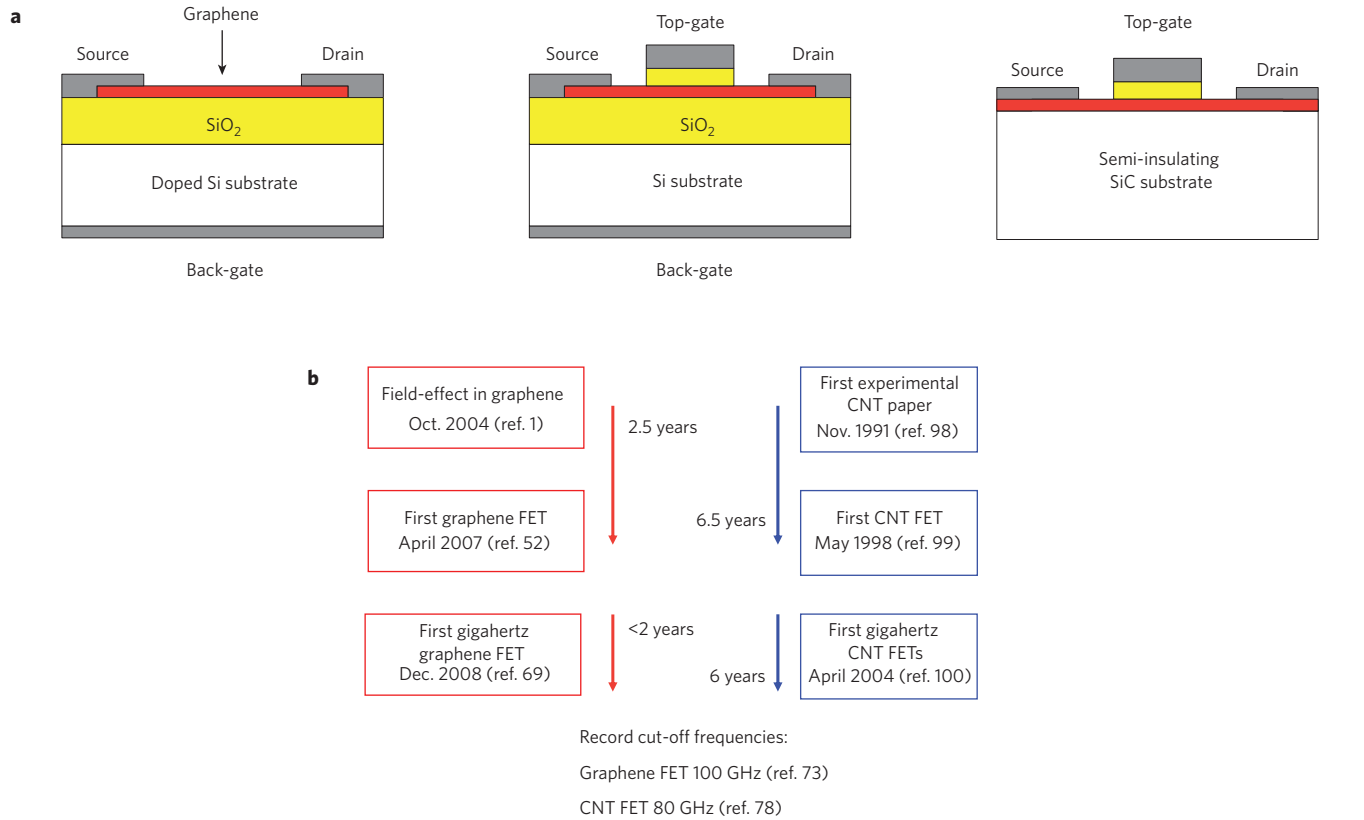


**Figure 6 | Structure and evolution of graphene MOSFETs. a**, Schematics of different graphene MOSFET types: back-gated MOSFET (left); top-gated MOSFET with a channel of exfoliated graphene or of graphene grown on metal and transferred to a $SiO_2$-covered Si wafer (middle); top-gated MOSFET with an epitaxial-graphene channel (right). The channel shown in red can consist of either large-area graphene or graphene nanoribbons. **b**, Progress in graphene MOSFET development[1,52,69,73] compared with the evolution of nanotube FETs[78,98–100].

definitions for the MOSFET channel mobility and they are difficult to compare[66]. Furthermore, the techniques used to measure mobility are only vaguely described in some papers. Most frequently, the field-effect mobility, $\mu_{FE}$, is measured (Table 1). However, the effect of the source and drain series resistances must be eliminated from the measured characteristics to determine this quantity, and it is not always clear that this has been done.

An additional complication lies in the interpretation of data from top-gated graphene MOSFETs, which involves arriving at a value for the gate capacitance, $C_G$. Frequently $C_G$ is approximated by the oxide capacitance per unit area, as $C_{ox} = \varepsilon_{ox}/t_{ox}$, where $\varepsilon_{ox}$ is the dielectric constant of the top-gate dielectric and $t_{ox}$ is the thickness of this dielectric. However, when $t_{ox}$ is small, the quantum capacitance, $C_q$, must be taken into account[67,68] because it is connected in series with $C_{ox}$, making the overall gate capacitance $C_G = C_{ox}C_q/(C_{ox} + C_q)$. The overall gate capacitance can be significantly smaller than $C_{ox}$, particularly close to the Dirac point (the point of minimum drain current), so neglecting the effect of $C_q$ will lead to an underestimate of the field-effect mobility.

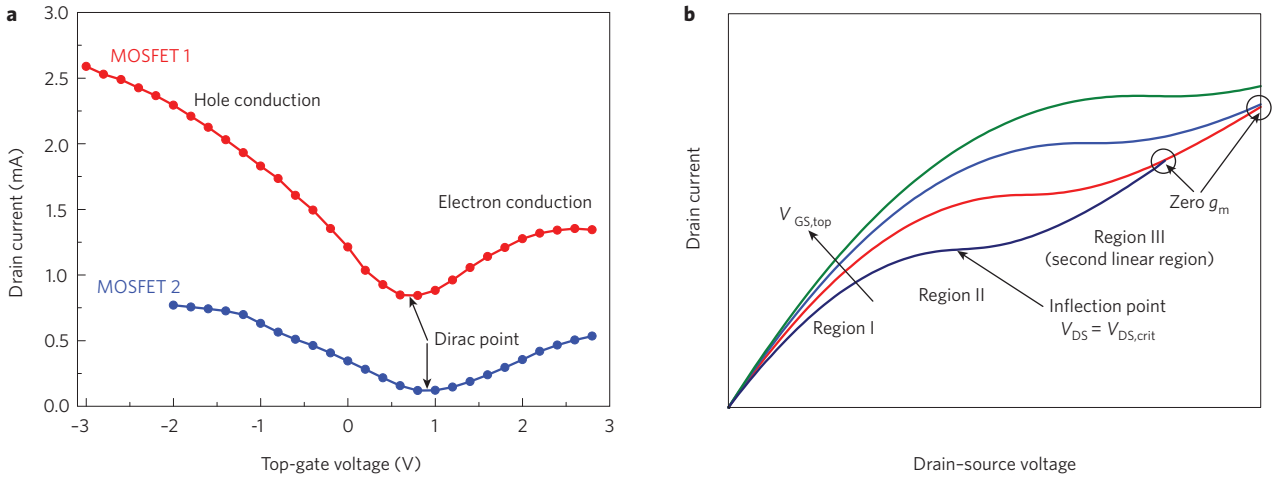


**Figure 7 | Direct-current behaviour of graphene MOSFETs with a large-area-graphene channel. a**, Typical transfer characteristics for two MOSFETs with large-area-graphene channels[23,71]. The on–off ratios are about 3 (MOSFET 1) and 7 (MOSFET 2), far below what is needed for applications in logic circuits. Unlike conventional Si MOSFETs, current flows for both positive and negative top-gate voltages. **b**, Qualitative shape of the output characteristics (drain current, $I_D$, versus drain–source voltage, $V_{DS}$) of a MOSFET with an n-type large-area-graphene channel, for different values of the top-gate voltage, $V_{GS,top}$. Saturation behaviour can be seen. At sufficiently large $V_{DS}$ values, the output characteristics for different $V_{GS,top}$ values may cross[75], leading to a zero or even negative transconductance, which means that the gate has effectively lost control of the current.

## State of the art of graphene transistors

A graphene MOS device was among the breakthrough results reported by the Manchester group in 2004 (ref. 1). A 300-nm $SiO_2$ layer underneath the graphene served as a back-gate dielectric and a doped silicon substrate acted as the back-gate (Fig. 6a). Such back-gate devices have been very useful for proof-of-concept purposes, but they suffer from unacceptably large parasitic capacitances and cannot be integrated with other components. Therefore, practical graphene transistors need a top-gate. The first graphene MOSFET with a top-gate was reported in 2007 (ref. 52), representing an important milestone, and progress has been very rapid since then (Fig. 6b). Although research into graphene is still in its infancy, graphene MOSFETs can compete with devices that have benefited from decades of research and investment.

Top-gated graphene MOSFETs have been made with exfoliated graphene[52–55,69,70], graphene grown on metals such as nickel and copper[71,72], and epitaxial graphene[23,73,74]; $SiO_2$, $Al_2O_3$, and $HfO_2$ have been used for the top-gate dielectric. The channels of these top-gated graphene transistors have been made using large-area graphene, which does not have a bandgap, so they have not been able to switch off.

Large-area-graphene transistors have a unique current–voltage transfer characteristic (Fig. 7a). The carrier density and the type of carrier (electrons or holes) in the channel are governed by the potential differences between the channel and the gates (top-gate and/or back-gate). Large positive gate voltages promote an electron accumulation in the channel (n-type channel), and large negative gate voltages lead to a p-type channel. This behaviour gives rise to the two branches of the transfer characteristics separated by the Dirac point (Fig. 7a). The position of the Dirac point depends on several factors: the difference between the work functions of the gate and the graphene, the type and density of the charges at the interfaces at the top and bottom of the channel (Fig. 6), and any doping of the graphene. The on–off ratios reported for MOSFET devices with large-area-graphene channels are in the range 2–20.

The output characteristics of many graphene MOSFETs either show a linear shape without any saturation[53] or only weak saturation[73,74], each of which is a disadvantage with respect to device speed. However, some graphene MOSFETs have an unusual form of saturation-like behaviour that includes a second linear region[70,71,75] (Fig. 7b). Our present understanding of the origin of this behaviour is as follows. For small values of $V_{DS}$, the transistor operates in the linear region and the entire channel is n-type (region I). As $V_{DS}$ is increased, the drain current starts to saturate until the inflection point at $V_{DS} = V_{DS,crit}$ is reached (region II). At this point, the potential conditions at the drain end of the channel correspond to the Dirac point. Once $V_{DS}$ exceeds $V_{DS,crit}$, the conduction type at the drain end of the channel switches from n-type to p-type[70,76] and the transistor enters a second linear region (region III). At sufficiently large values of $V_{DS}$, the output characteristics for different gate voltages may cross[75], leading to a zero or even negative transconductance—a highly undesirable situation. This peculiar behaviour is a consequence of these devices having gapless channels and does not occur in FETs with semiconducting channels.

Recently, graphene MOSFETs with gigahertz capabilities have been reported. These transistors possess large-area channels of exfoliated[53,55,69,77] and epitaxial[73,74] graphene. The fastest graphene transistor currently is a MOSFET with a 240-nm gate that has a cut-off frequency of $f_T$ = 100 GHz (ref. 73), which is higher than those of the best silicon MOSFETs with similar gate lengths (as is the cut-off frequency of 53 GHz reported for a device with a 550-nm gate, also in ref. 73). A weak point of all radiofrequency graphene MOSFETs reported so far is the unsatisfying saturation behaviour (only weak saturation or the second linear regime), which has an adverse impact on the cut-off frequency, the intrinsic gain and other figures of merit for radiofrequency devices. However, outperforming silicon MOSFETs while operating with only weak current saturation[73] is certainly impressive.

Figure 8 shows the cut-off frequency for a variety of devices including graphene MOSFETs, nanotube FETs, and various radiofrequency FETs. For conventional radiofrequency FETs with gate lengths greater than 0.2 μm, the $f_T$ data for each transistor type has an $L^{-1}$ dependence, where $L$ is the gate length. Furthermore, $f_T$ increases with mobility[9]. Silicon MOSFETs show channel mobilities of a few 100 $cm^2\ V^{-1}\ s^{-1}$ compared with about 6,000 $cm^2\ V^{-1}\ s^{-1}$ for GaAs pHEMTs and more than 10,000 $cm^2\ V^{-1}\ s^{-1}$ for InP HEMTs and GaAs mHEMTs. At shorter gate lengths, however, the mobility becomes less important for transistor speed and the deleterious influence of parasitic resistances and short-channel effects increases. Both nanotube and graphene FETs are still slower than

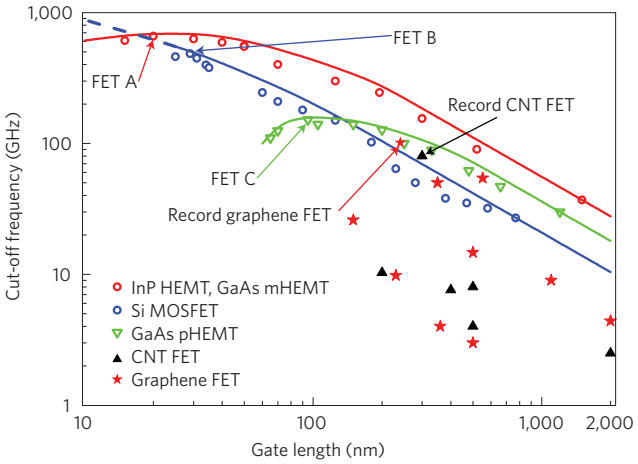


**Figure 8 | Comparing cut-off frequencies for different FETs.** Cut-off frequency versus gate length for graphene MOSFETs, nanotube FETs and three types of radiofrequency FET; the symbols are experimental data points and the lines are a guide to the eye for type A (InP HEMT and GaAs mHEMT), B (Si MOSFET) and C (GaAs pHEMT) devices (as indicated). The FET A with the highest cut-off frequency (660 GHz) is a GaAs metamorphic HEMT (mHEMT) with a 20-nm gate (M. Schlechtweg, personal communication). The FET B with the highest cut-off frequency (485 GHz) is a Si MOSFET with a 29-nm gate[101]. The FET C with the highest cut-off frequency (152 GHz) is a GaAs pseudomorphic HEMT (pHEMT) with a 100-nm gate[102]. The fastest nanotube device (CNT FET) has $f_T$ = 80 GHz and $L$ = 300 nm (ref. 78), and the fastest reported graphene MOSFET has $f_T$ = 100 GHz and $L$ = 240 nm (ref. 73).

the best conventional radiofrequency FETs, but they have recently overtaken the best silicon MOSFETs with gate lengths above 200 nm and are approaching the performance of GaAs pHEMTs. (See ref. 78 for details of the nanotube with the highest $f_T$ reported so far, and ref. 79 for more information on the radiofrequency potential of nanotube FETs.)

Although the low on–off ratios demonstrated so far make use in logic devices unrealistic, transistors with large-area graphene channels are promising candidates for radiofrequency applications because radiofrequency FETs are not required to switch off and can benefit from the high mobilities offered by large-area graphene. However, the absence of drain-current saturation will limit the radiofrequency performance of graphene transistors.

One method of introducing a bandgap into graphene for logic applications is to create graphene nanoribbons. Nanoribbon MOSFETs with back-gate control and widths down to less than 5 nm have been operated as p-channel devices and had on–off ratios of up to $10^6$ (refs 26,62). Such high ratios have been obtained despite simulations showing that edge disorder leads to an undesirable decrease in the on-currents and a simultaneous increase in the off-current of nanoribbon MOSFETs[80,81].This, and other evidence of a sizeable bandgap opening in narrow nanoribbons, provides proof of the suitability of nanoribbon FETs for logic applications. However, these devices had relatively thick back-gate oxides, so voltage swings of several volts were needed for switching, which is significantly more than the swings of 1 V and less needed to switch Si CMOS devices[2]. Furthermore, CMOS logic requires both n-channel and p-channel FETs with well-controlled threshold voltages, and graphene FETs with all these properties have not yet been reported.

Recently, the first graphene nanoribbon MOSFETs with top-gate control have been reported[82]. These transistors feature a thin high-dielectric-constant (high-$k$) top-gate dielectric (1–2 nm of $HfO_2$), a room-temperature on–off ratio of 70 and an outstanding transconductance of 3.2 mS $\mu m^{-1}$ (which is higher than the transconductances reported for state-of-the-art silicon MOSFETs and III–V HEMTs).

Graphene bilayer MOSFETs have been investigated experimentally[83] and by device simulation[84]. Although the on–off ratios reported so far (100 at room temperature and 2,000 at low temperature[83]) are too small for logic applications, they mark a significant improvement (of about a factor of 10) over MOSFETs in which the channel is made of large-area gapless graphene.

The contact resistance between the metallic source and drain contacts and the graphene channel should be briefly mentioned. So far, the lowest reported metal–graphene contact resistances are in the range 500–1,000 Ω cm (refs 85,86), which is about ten times the contact resistance of silicon MOSFETs and III–V HEMTs[8,13]. Remarkably, in spite of the importance of the contacts (particularly for short-channel devices), only a few studies dealing with metal–graphene contacts have been published[85–87] and more work is needed to understand the contact properties.

I now return to the two-dimensional nature of graphene. According to scaling theory, as noted previously, a thin channel region allows short-channel effects to be suppressed and thus makes it feasible to scale MOSFETs to very short gate lengths. The two-dimensional nature of graphene means it offers us the thinnest possible channel, so graphene MOSFETs should be more scalable than their competitors. It should be noted, however, that scaling theory is valid only for transistors with a semiconducting channel and does not apply to graphene MOSFETs with gapless channels. Thus, the scaling theory does describe nanoribbon MOSFETs, which have a bandgap but which have significantly lower mobilities than large-area graphene, as discussed. Given that the high published values of mobility relate to gapless large-area graphene, the most attractive characteristic of graphene for use in MOSFETs, in particular those required to switch off, may be its ability to scale to shorter channels and higher speeds, rather than its mobility.

## Further options for graphene devices

It has become clear that graphene devices based on the conventional MOSFET principle suffer from some fundamental problems. This has motivated researchers to explore new graphene device concepts, such as tunnel FETs and bilayer pseudospin FETs. In a tunnel FET, the band-to-band tunnelling across the source–channel junction can be controlled using the gate–source voltage. The big advantage of tunnel FETs is that their subthreshold swings are not limited to 60 mV per decade, as in conventional MOSFETs[7,10], which should lead to steeper subthreshold characteristics and better switch-off. The tunnel-FET approach has already been explored in silicon and carbon-nanotube MOSFETs[88,89]. Tunnel FETs based on nanoribbons and bilayer graphene have been investigated in simulations[84,90,91] but have not been demonstrated experimentally. In particular, the bilayer graphene tunnel FET is now considered to be a promising device for a number of reasons: narrow nanoribbons are not needed, so edge disorder will not be a problem and patterning will be relatively easy; the small bandgap opened by a vertical field applied across the two layers is sufficient to suppress band-to-band tunnelling in the off-state and thus enables effective switch-off; and the possibility of subthreshold swings below 60 mV per decade should make high on–off ratios possible[84].

The bilayer pseudospin FET consists of a vertical stack of two graphene layers separated by a thin dielectric[92]. Under certain bias conditions the tunnelling resistance between the two graphene layers becomes so small that the layers are effectively shorted, causing the FET to pass a high current, whereas under other conditions the tunnelling resistance is very large, shutting the current off. The bilayer pseudospin FET might therefore be able to deliver fast and ultralow-power logic operation.

Although graphene tunnel FETs and bilayer pseudospin FETs are both still at an embryonic stage, they have already gained considerable attention in the electron-device community and have been included in the chapter on emerging research devices in the latest edition of the ITRS[2]. It might also be possible to make interconnects from graphene, which would open the possibility of all-graphene integrated circuits in which both the active devices and the wiring were made of graphene[22]. It has been shown that graphene interconnects compete well with copper interconnects[93,94]; indeed, graphene can support current densities greater than $10^8$ A cm$^{-2}$ (which is 100 times higher than those supported by copper and is comparable with those supported by nanotubes)[95] and has a thermal conductivity of around 30–50 W cm$^{-1}$ K$^{-1}$ (in comparison with 4 W cm$^{-1}$ K$^{-1}$ for copper)[96].

## Outlook

Since 2007, we have witnessed huge progress in the development of graphene transistors. Most impressive were the demonstrations of a graphene MOSFET with a cut-off frequency of 100 GHz (ref. 73), the excellent switching behaviour of nanoribbon MOSFETs[26,62], and channel mobilities exceeding 20,000 cm$^2$ V$^{-1}$ s$^{-1}$ in top-gated graphene MOSFETs[54]. However, this progress has been accompanied by the appearance of a number of problems. MOSFETs with large-area-graphene channels cannot be switched off, making them unsuitable for logic applications, and their peculiar saturation behaviour limits their radiofrequency performance. Nanoribbon graphene, which does have a bandgap and results in transistors that can be switched off, has serious fabrication issues because of the small widths required and the presence of edge disorder.

The primary challenges facing the community at present, therefore, are to create in a controlled and practical fashion a bandgap in graphene, which would allow logic transistors to switch off and radiofrequency transistors to avoid the second linear regime (Fig. 7b), and to develop other means of improving transistor saturation characteristics by, for example, developing contacts that block one kind of carrier without degrading the transistor's speed. The community may also benefit from recognizing that the motivation to use graphene in transistors in the first place stems less from ultrahigh mobilities than from graphene's ability to scale to short gate lengths and high speeds by virtue of its thinness.

This discussion of the problems of graphene MOSFETs should not lead to the conclusion that graphene is not a promising material for transistors. Rather, I have chosen a more critical view to avoid a situation that has been seen in the past, in which a new device or material concept has been prematurely declared capable of replacing the status quo. Also, I agree with David Ferry, a veteran of semiconductor device research, when he says that[97] "many such saviours have come and gone, yet the reliable silicon CMOS continues to be scaled and to reach even higher performance levels".

I conclude by noting that the first top-gated graphene transistors were reported only three years ago. Given this short history, and given that all other possible successors to conventional mainstream transistors also face serious problems, we cannot help but be impressed with the rapid development of graphene. Concepts that have been investigated for many years, such as spin transistors or molecular devices, seem to be farther from real application than does graphene, and it is not clear if they will ever reach the production stage. At the moment, it is impossible to say which, if any, of the alternative device concepts being considered will replace conventional transistors. However, the latest ITRS roadmap strongly recommends intensified research into graphene and even contains a research and development schedule for carbon-based nanoelectronics[2]. The race is still open and the prospects for graphene devices are at least as promising as those for alternative concepts.

## References


1. Novoselov, K. S. *et al.* Electric field effect in atomically thin carbon films. *Science* **306,** 666–669 (2004).
2. *The International Technology Roadmap for Semiconductors* http://www.itrs.net/Links/2009ITRS/Home2009.htm (Semiconductor Industry Association, 2009).
3. Geim, A. K. & Novoselov, K. S. The rise of graphene. *Nature Mater.* **6,** 183–191 (2007).
4. Geim, A. K. Graphene: status & prospects. *Science* **324,** 1530–1534 (2009).
5. Castro Neto, A. H. *et al.* The electronic properties of graphene. *Rev. Mod. Phys.* **81,** 109–162 (2009).
6. Moore, G. E. in *Tech. Dig. ISSCC* 20–23 (IEEE, 2003).
7. Schwierz, F., Wong, H. & Liou, J. J. *Nanometer CMOS* (Pan Stanford, 2010).
8. Schwierz, F. & Liou, J. J. *Modern Microwave Transistors – Theory, Design, and Performance* (Wiley, 2003).
9. Schwierz, F. & Liou, J. J. RF transistors: recent developments and roadmap toward terahertz applications. *Solid-State Electron.* **51,** 1079–1091 (2007).
10. Taur, Y. & Ning, T. H *Fundamentals of Modern VLSI Devices* (Cambridge Univ. Press, 1998).
11. Frank, D. J., Taur, Y. & Wong, H-S. P. Generalized scale length for two-dimensional effects in MOSFETs. *IEEE Electron Dev. Lett.* **19,** 385–387 (1998).
12. Aberg, I. & Hoyt, J. L. Hole transport in ultra-thin-body MOSFETs in strained-Si directly on insulator with strained-Si thickness less than 5 nm. *IEEE Electron Dev. Lett.* **26,** 661–663 (2005).
13. Thompson, S. E. *et al.* In search of "forever", continued transistor scaling one new material at a time. *IEEE Trans. Semicond. Manuf.* **18,** 26–36 (2005).
14. Uyemura, J. P. *CMOS Logic Circuit Design* (Kluwer Academic, 1999).
15. Hughes, B. & Tasker, P. J. Bias dependence of the MODFET intrinsic model elements values at microwave frequencies. *IEEE Trans. Electron. Dev.* **36,** 2267–2273 (1989).
16. Nguyen, L. D. *et al.* in *Tech. Dig. IEDM* 176–179 (IEEE, 1988).
17. Boehm, H. P., Clauss, A., Hofmann, U. & Fischer, G. O. Dünnste Kohlenstoff-Folien. *Z. Naturforsch. B* **17,** 150–153 (1962).
18. May, J. W. Platinum surface LEED rings. *Surf. Sci.* **17,** 267–270 (1969).
19. van Bommel, A. J., Crombeen, J. E. & van Tooren, A. LEED and Auger electron observations of the SiC (0001) surface. *Surf. Sci.* **48,** 463–472 (1975).
20. Kim, K-S. *et al.* Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature* **457,** 706–710 (2009).
21. Reina, A. *et al.* Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition. *Nano Lett.* **9,** 30–35 (2009).
22. Berger, C. *et al.* Electronic confinement and coherence in patterned epitaxial graphene. *Science* **312,** 1191–1196 (2006).
23. Kedzierski, J. *et al.* Epitaxial graphene transistors on SiC substrates. *IEEE Trans. Electron. Dev.* **55,** 2078–2085 (2008).
24. Han, M. *et al.* Energy band-gap engineering of graphene nanoribbons. *Phys. Rev. Lett.* **98,** 206805 (2007).
25. Kim, P. *et al.* in *Tech. Dig. IEDM* 241–244 (IEEE, 2009).
26. Li, X., Wang, X., Zhang, L., Lee, S. & Dai, H. Chemically derived, ultrasmooth graphene nanoribbon semiconductors. *Science* **319,** 1229–1232 (2008).
27. Chen, Z., Lin, Y-M., Rooks, M. J. & Avouris, Ph. Graphene nano-ribbon electronics. *Physica E* **40,** 228–232 (2007).
28. Yang, L. *et al.* Quasiparticle energies and band gaps in graphene nanoribbons. *Phys. Rev. Lett.* **99,** 186801 (2007).
29. Evaldsson, M., Zozoulenko, I. V., Xu, H. & Heinzel, T. Edge-disorder-induced Anderson localization and conduction gap in graphene nanoribbons. *Phys. Rev. B* **78,** 161407 (2008).
30. Castro, E. V. *et al.* Biased bilayer graphene: semiconductor with a gap tunable by the electric field effect. *Phys. Rev. Lett.* **99,** 216802 (2007).
31. Gava, P., Lazzeri, M., Saitta, A. M. & Mauri, F. *Ab initio* study of gap opening and screening effects in gated bilayer graphene. *Phys. Rev. B* **79,** 165431 (2009).
32. Ohta, T., Bostwick, A., Seyller, Th., Horn, K. & Rotenberg, E. Controlling the electronic structure of bilayer graphene. *Science* **313,** 951–954 (2006).
33. Zhang, Y. *et al.* Direct observation of a widely tunable bandgap in bilayer graphene. *Nature* **459,** 820–823 (2009).
34. Rotenberg, E. *et al.* and Zhou, S. Y. *et al.* Origin of the energy bandgap in epitaxial graphene. *Nature Mater.* **7,** 258–260 (2008).
35. Zhou, S. Y. *et al.* Substrate-induced bandgap opening in epitaxial graphene. *Nature Mater.* **6,** 770–775 (2007).
36. Kim, S., Ihm, J., Choi, H. J. & Son, Y-W. Origin of anomalous electronic structures of epitaxial graphene on silicon carbide. *Phys. Rev. Lett.* **100,** 176802 (2008).
37. Bostwick, A., Ohta, T., Seyller, Th., Horn, K. & Rotenberg, E. Quasiparticle dynamics in graphene. *Nature Phys.* **3,** 36–40 (2007).
38. Peng, X. & Ahuja, R. Symmetry breaking induced bandgap in epitaxial graphene layers on Si. *Nano Lett.* **8,** 4464–4468 (2008).
39. Sano, E. & Otsuji, T. Theoretical evaluation of channel structure in graphene field-effect transistors. *Jpn. J. Appl. Phys.* **48,** 041202 (2009).
40. Pereira, V. M., Castro Neto, A. H. & Peres, N. M. R. Tight-binding approach to uniaxial strain in graphene. *Phys. Rev. B* **80,** 045401 (2009).

41. Ni, Z. H. *et al.* Uniaxial strain on graphene: Raman spectroscopy study and band-gap opening. *ACS Nano* **2,** 2301–2305 (2008); erratum **3,** 483 (2009).
42. Sols, F., Guinea, F. & Castro Neto, A. H. Coulomb blockade in graphene nanoribbons. *Phys. Rev. Lett.* **99,** 166803 (2007).
43. Han, M. Y., Brant, J. C. & Kim, P. Electron transport in disordered graphene nanoribbons. *Phys. Rev. Lett.* **104,** 056801 (2010).
44. Cervantes-Sodi, F., Csanyi, G., Picanec, S. & Ferrari, A. C. Edge-functionalized and substitutionally doped graphene nanoribbons: electronic and spin properties. *Phys. Rev. B* **77,** 165427 (2008).
45. Jiao, J., Wang, X., Diankov, G., Wang, H. & Dai, H. Facile synthesis of high-quality graphene nanoribbons. *Nature Nanotech.* **5,** 321–325 (2010).
46. Raza, H. & Kan, E. C. Armchair graphene nanoribbons: electronic structure and electric-field modulation. *Phys. Rev. B* **77,** 245434 (2008).
47. Chen, J-H., Jang, C., Xiao, S., Ishigami, M. & Fuhrer, M. S. Intrinsic and extrinsic performance limits of graphene devices on $SiO_2$. *Nature Nanotech.* **3,** 206–209 (2008).
48. Chen, F., Xia, J., Ferry, D. K. & Tao, N. Dielectric screening enhanced performance in graphene FET. *Nano Lett.* **9,** 2571–2574 (2009).
49. Morozov, V. S. *et al.* Giant intrinsic carrier mobilities in graphene and its bilayer. *Phys. Rev. Lett.* **100,** 016602 (2008).
50. Geim, A. Graphene update. *Bull. Am. Phys. Soc.* **55,** abstr. J21.0004, http://meetings.aps.org/link/BAPS.2010.MAR.J21.4 (2010).
51. Emtsev, K. V. *et al.* Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. *Nature Mater.* **8,** 203–207 (2009).
52. Lemme, M. C., Echtermeyer, T. J., Baus, M. & Kurz, H. A graphene field-effect device. *IEEE Electron Dev. Lett.* **28,** 282–284 (2007).
53. Lin, Y-M. *et al.* Operation of graphene transistors at gigahertz frequencies. *Nano Lett.* **9,** 422–426 (2009).
54. Liao, L. *et al.* High-$\kappa$ oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors. *Proc. Natl Acad. Sci. USA* **107,** 6711–6715 (2010).
55. Farmer, D. B. *et al.* Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors. *Nano Lett.* **9,** 4474–4478 (2009).
56. Zhou, X., Park, J-Y., Huang, S., Liu, J. & McEuen, P. L. Band structure, phonon scattering, and performance limit of single-walled carbon nanotube transistors. *Phys. Rev. Lett.* **95,** 146805 (2005).
57. Perebeinos, V., Tersoff, J. & Avouris, Ph. Electron-phonon interaction and transport in semiconducting carbon nanotubes. *Phys. Rev. Lett.* **94,** 0786802 (2005).
58. Obradovic, B. *et al.* Analysis of graphene nanoribbons as a channel material for field-effect transistors. *Appl. Phys. Lett.* **88,** 142102 (2006).
59. Fang, T., Konar, A., Xing, H. & Jena, D. Mobility in semiconducting nanoribbons: phonon, impurity, and edge roughness scattering. *Phys. Rev. B* **78,** 205403 (2008).
60. Bresciani, M., Palestri, P., Esseni, D. & Selmi, L. in *Proc. ESSDERC '09* 480–483 (IEEE, 2009).
61. Betti, A., Fiori, G., Iannaccone, G. & Mao, Y. in *Tech. Dig. IEDM 2009* 897–900 (IEEE, 2009).
62. Wang, X. *et al.* Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors. *Phys. Rev. Lett.* **100,** 206803 (2008).
63. Akturk, A. & Goldsman, N. Electron transport and full-band electron-phonon interactions in graphene. *J. Appl. Phys.* **103,** 053702 (2008).
64. Shishir, R. S. & Ferry, D. K. Velocity saturation in intrinsic graphene. *J. Phys. Condens. Matter* **21,** 344201 (2009).
65. Barreiro, A., Lazzeri, M., Moser, J., Mauri, F. & Bachtold, A. Transport properties of graphene in the high-current limit. *Phys. Rev. Lett.* **103,** 076601 (2009).
66. Schroder, D. K. *Semiconductor Material and Device Characterization* (Wiley, 1990).
67. Fang, T., Konar, A., Xing, H. & Jena, D. Carrier statistics and quantum capacitance of graphene sheets and nanoribbons. *Appl. Phys. Lett.* **91,** 092109 (2007).
68. Chen, Z. & Appenzeller, J. in *Tech. Dig. IEDM 2008*, paper 21.1 (IEEE, 2008).
69. Meric, I., Baklitskaya, N., Kim, P. & Shepard, K. L. in *Tech. Dig. IEDM 2008*, paper 21.2 (IEEE, 2008).
70. Meric, I. *et al.* Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nature Nanotech.* **3,** 654–659 (2008).
71. Kedzierski, J. *et al.* Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition. *IEEE Electron Dev. Lett.* **30,** 745–747 (2009).
72. Li, X. *et al.* Large-area synthesis of high-quality and uniform graphene films on copper foils. *Science* **324,** 1312–1314 (2009).
73. Lin, Y-M. *et al.* 100-GHz transistors from wafer-scale epitaxial graphene. *Science* **327,** 662 (2010).
74. Moon, J. S. *et al.* Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates. *IEEE Electron Dev. Lett.* **30,** 650–652 (2009).
75. Tahy, K. *et al.* in *Proc. Dev. Res. Conf. 2009* 207–208 (IEEE, 2009).
76. Thiele, S., Schaefer, J. A. & Schwierz, F. Modeling of graphene metal–oxide–semiconductor field-effect transistors with gapless large-area graphene channels. *J. Appl. Phys.* **107,** 094505 (2010).
77. Lin, Y-M. *et al.* Dual-gate graphene FETs with $f_T$ of 50 GHz. *IEEE Electron Dev. Lett.* **31,** 68–70 (2010).
78. Nougaret, N. *et al.* 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes. *Appl. Phys. Lett.* **94,** 243505 (2009).
79. Rutherglen, C., Jain, D. & Burke, P. Nanotube electronics for radiofrequency applications. *Nature Nanotech.* **4,** 811–819 (2009).
80. Yoon, Y. & Guo, J. Effects of edge roughness in graphene nanoribbon transistors. *Appl. Phys. Lett.* **91,** 073103 (2007).
81. Basu, D., Gilbert, M. J., Register, L. F., Banerjee, S. K. & MacDonald, A. H. Effect of edge roughness on electronic transport in graphene nanoribbon channel metal–oxide–semiconductor field-effect transistors. *Appl. Phys. Lett.* **92,** 042114 (2008).
82. Liao, L. *et al.* Top-gated graphene nanoribbon transistors with ultrathin high-*k* dielectrics. *Nano Lett.* **10,** 1917–1921 (2010).
83. Xia, F., Farmer, D. B., Lin, Y-M. & Avouris, Ph. Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. *Nano Lett.* **10,** 715–718 (2010).
84. Iannaccone, G. *et al.* in *Tech. Dig. IEDM 2009* 245–248 (IEEE, 2009).
85. Nagashio, K., Nishimura, T., Kita, K. & Toriumi, A. in *Tech. Dig. IEDM 2009* 565–568 (IEEE, 2009).
86. Russo, S., Cracuin, M. F., Yamamoto, Y., Morpurgo, A. F. & Tarucha, S. Contact resistance in graphene-based devices. *Physica E* **42,** 677–679 (2010).
87. Huard, B., Stander, N., Sulpizio, J. A. & Goldhaber-Gordon, D. Evidence of the role of contacts on the observed electron-hole asymmetry in graphene. *Phys. Rev. B* **78,** 121402 (2008).
88. Boucart, K. & Ionescu, A. M. Double-gate tunnel FET with high-$\kappa$ gate dielectric. *IEEE Trans. Electron. Dev.* **54,** 1725–1733 (2007).
89. Appenzeller, J., Lin, Y-M., Knoch, J. & Avouris, Ph. Band-to-band tunneling in carbon nanotube field-effect transistor. *Phys. Rev. Lett.* **93,** 196805 (2004).
90. Luisier, M. & Klimeck, G. in *Proc. Dev. Res. Conf. 2009* 201–202 (IEEE, 2009).
91. Fiori, G. & Iannaccone, G. Ultralow-voltage bilayer graphene tunnel FET. *IEEE Electron Dev. Lett.* **30,** 1096–1098 (2009).
92. Banerjee, S. K., Register, L. F., Tutuc, E., Reddy, D. & MacDonald, A. H. Bilayer pseudospin field-effect transistor (BiSFET): a proposed new logic device. *IEEE Electron Dev. Lett.* **30,** 158–160 (2009).
93. Murali, R., Brenner, K., Yang, Y., Beck, Th. & Meindl, J. D. Resistivity of graphene nanoribbon interconnects. *IEEE Electron Dev. Lett.* **30,** 611–613 (2009).
94. Awano, Y. in *Tech. Dig. IEDM 2009* 233–236 (IEEE, 2009).
95. Moser, J., Barreiro, A. & Bachtold, A. Current-induced cleaning of graphene. *Appl. Phys. Lett.* **91,** 163513 (2007).
96. Balandin, A. A. *et al.* Superior thermal conductivity of single-layer graphene. *Nano Lett.* **8,** 902–907 (2008).
97. Ferry, D. K., Gilbert, M. J. & Akis, R. Some considerations on nanowires in nanoelectronics. *IEEE Trans. Electron. Dev.* **55,** 2820–2826 (2008).
98. Iijima, S. Helical microtubules of graphitic carbon. *Nature* **354,** 56–58 (1991).
99. Tans, S. J., Verschueren, A. R. M. & Dekker, C. Room-temperature transistor based on a single carbon nanotube. *Nature* **393,** 49–52 (1998).
100. Li, S., Yu, Z., Yen, S-F., Tang, W. C. & Burke, P. J. Carbon nanotube transistor operation at 2.6 GHz. *Nano Lett.* **4,** 753–756 (2004).
101. Lee, S. *et al.* in *Tech. Dig. IEDM 2007* 255–258 (IEEE, 2007).
102. Nguyen, L. D., Tasker, P. J., Radulescu, D. C. & Eastman, L. F. Characterization of ultra-high-speed AlGaAs/InGaAs (on GaAs) MODFETs. *IEEE Trans. Electron. Dev.* **36,** 2243–2248 (1989).


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## Additional information

The authors declare no competing financial interests.